List of Common Symbols and Abbreviations

Only the symbols and abbreviations which are used commonly throughout this thesis are defined here. A more detailed list of symbols and abbreviations are defined separately at the beginning of each chapter.

Δ	Maximum Vertex Degree of a Bi-partite Graph
B	Leaky Bucket Size
b	Memory Block Size
$c,\ C$	Cell, Number of Copies
DT	Departure Time
E	Number of State Entries
k	Number of memories, PPS layers
L	Latency between Scheduler Request and Buffer Response
M	Total Number of Memories
m	Multicast Fanout
N	Number of Ports of a Router, Counters
Q	Number of Queues
q	Number of Multicast Copies
R	Line Rate
RTT	Round Trip Time
S	Speedup
T	Time Slot
T_{RC}	Random Cycle Time of Memory
x	Pipeline Look-ahead
ASIC	Application Specific Integrated Circuit
ATM	Asynchronous Transfer Mode

CAM	Content Addressable Memory
CIOQ	Combined Input Output Queued
CMA	Counter Management Algorithm
CMOS	Complementary Metal–Oxide–Semiconductor
CPA	Centralized Parallel Packet Switch Algorithm
CSM	Centralized Shared Memory Router
DDoS	Distributed Denial of Service
DDR	Double Data Rate
DPA	Distributed Parallel Packet Switch Algorithm
DRAM	Dynamic Random Access Memory
DRR	Deficit Round Robin
DSM	Distributed Shared Memory Router
DWDM	Dense Wavelength Division Multiplexing
ECC	Error Correcting Codes
ECQF	Earliest Critical Queue First
eDRAM	Embedded Dynamic Random Access Memory
FCFS	First Come First Serve (same as FIFO)
FCRAM	Fast Cycle Random Access Memory
FIFO	First In First Out Queue
GPS	Generalized Processor Sharing
HoL	Head of Line
IP	Internet Protocol
IQ	Input Queued Router
ISP	Internet Service Provider
LAN	Local Area Network
LCF	Longest Counter First

MAC	Media Access Controller
MDQF	Most Deficited Queue First
MDQFP	Most Deficited Queue First with Pipelining
MMA	Memory Management Algorithm
MWM	Maximum Weight Matching
NAT	Network Address Translation
OQ	Output Queued Router
PDSM	Parallel Distributed Shared Memory Router
PIFO	Push In First Out Queue
PIRO	Push In Random Out Queue
PPS	Parallel Packet Switch
PSM	Parallel Shared Memory Router
QDR	Quad Data Rate
QoS	Quality of Service
RAID	Redundant Array of Independent Disks
RDRAM	Rambus Dynamic Random Access Memory
RLDRAM	Reduced Latency Random Access Memory
SB	Single-buffered Router
SDRAM	Synchronous Dynamic Random Access Memory
SOHO	Small Office Home Office
SRAM	Static Random Access Memory
SVOQ	Super Virtual Output Queue
TCP	Transmission Control Protocol
TLB	Translation Lookaside Buffer
VoIP	Voice over Internet Protocol
VOQ	Virtual Output Queue

W^{2}FQ   Worst-Case Weighted Fair Queueing

WAN   Wide Area Network

WFA   Weighted Fair Arbiter

WFQ   Weighted Fair Queueing