"Good, Fast, Cheap: Pick any two
(you can't have all three)".
— RFC 1925, The Twelve Networking Truths[†]

A

Memory Terminology

In this appendix, we will define some common terms related to memory. The two most widespread memories available today are SRAM [2] and DRAM [3]. In what follows, we will define the DRAM memory terminology, of which SRAM terms are a subset.

A.1 Terminology

A DRAM's memory array is arranged internally in rows, where a set of contiguous rows form a bank. For example, Figure A.1 shows a DRAM with K banks, where each bank has R rows. The four key memory terms of concern to us are:

1. **Bandwidth:** This refers to the total amount of data that can be transferred from a single memory per unit time.
2. **Capacity:** This refers to the total number of bits that can be stored in the memory.
3. **Latency:** This refers to the time it takes to receive data from memory, after a request to access it has been issued by the requester.

[†]A more apt version for networking memories – "Dense, Fast, Cheap: Pick any two".

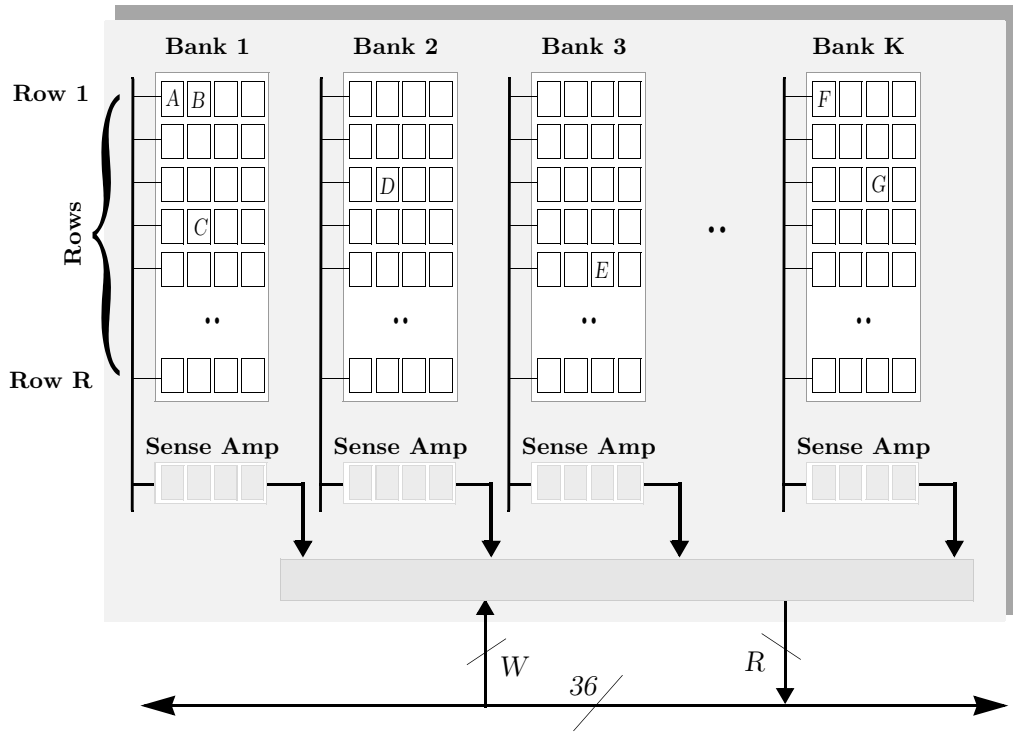

Figure A.1: *Internal architecture of a typical memory.*

4. **Access Time:** This refers to the minimum amount of time that needs to elapse between any two consecutive requests to the memory. The memory access time can depend on a number of factors, and this will be explained in the next section.

☞**Observation A.1.** Note that the memory bandwidth is a function of three quantities — (1) the data width of the memory, (2) the clock speed, and (3) the number of edges used per clock to transfer data. For example, a DRAM with a 36-bit data bus, running a 250 Mhz clock, which can support dual-data rate (DDR) transfer (*i.e.*, it can transfer data on both edges of the clock) has a bandwidth of $36 \times 250 \times 2 = 18$ Gb/s.

A.2 Access Time of a DRAM

The access time T of the DRAM (*i.e.*, the time taken between consecutive accesses to any location in the memory array) is dependent on the sequence of memory accesses made to the DRAM. These can be categorized as follows:

1. **Consecutive cells in the same row and bank:** The access time between two consecutive references to adjacent memory locations in the same row of the same bank is denoted by T_C. This is sometimes referred to as the burst mode in a DRAM. In Figure 2, consecutive references to cells A and B can be done in burst mode. T_C is usually about 5-10 ns today. Although this is fast, it is not common in a router to be able to use burst mode, because successive cells do not usually reside in the same row and bank.
2. **Consecutive cells in different rows, but in the same bank:** The access time between two consecutive references to different rows but belonging to the same bank is denoted by T_{RC}. As an example, consider the consecutive references to cells B and C in Figure A.1. We say that there is a *bank conflict*[1] because the rows being accessed belong to the same bank. T_{RC} represents the worst-case access time for random accesses to a DRAM, and it is of the order of 70-80ns for commodity DRAMs available today.
3. **Consecutive cells in adjacent banks:** Some DRAMs such as RDRAM [7] incur a penalty when two consecutive references are made to adjacent banks, *i.e.*, if a cell accesses bank x, then the next cell cannot access banks $x-1$, x, or $x+1$. This is called an *adjacent bank conflict*, and we will denote it by T_{AC}. This can occur if adjacent DRAM banks share circuitry, such as sense-amps. As an example, consecutive references to cells D and E in Figure A.1 cause an adjacent bank conflict. Most modern DRAMs do not share circuitry between adjacent banks, and hence do not exhibit adjacent bank conflicts.

[1]This is also commonly called a row conflict, however this terminology is misleading, since it is the banks that conflict, not the rows!

4. **Consecutive cells in different rows:** The access time for two consecutive references to rows in different banks is denoted by T_{RR} and is called the row to row access time. An example in Figure A.1 would be a reference to cell A, B, or C followed by a reference to cell D. This number is of the order of 20ns and usually represents the best-case random access time for a DRAM.

In a DRAM, there is usually a heavy penalty in the access time for a bank conflict.[2] Thus $T_{RC} \ll T_{RR}, T_{AC}$. In this thesis, when we mention random access time, we will refer to the worst-case random access time of the DRAM, *i.e.*, $T = \max\{T_{RC}, T_{RR}, T_{AC}\}$.

[2]Note that there can be other penalties such as the read-write turnaround and refresh penalties associated with accesses to a DRAM.