Algorithmic Memory Increases Memory Performance By an Order of Magnitude

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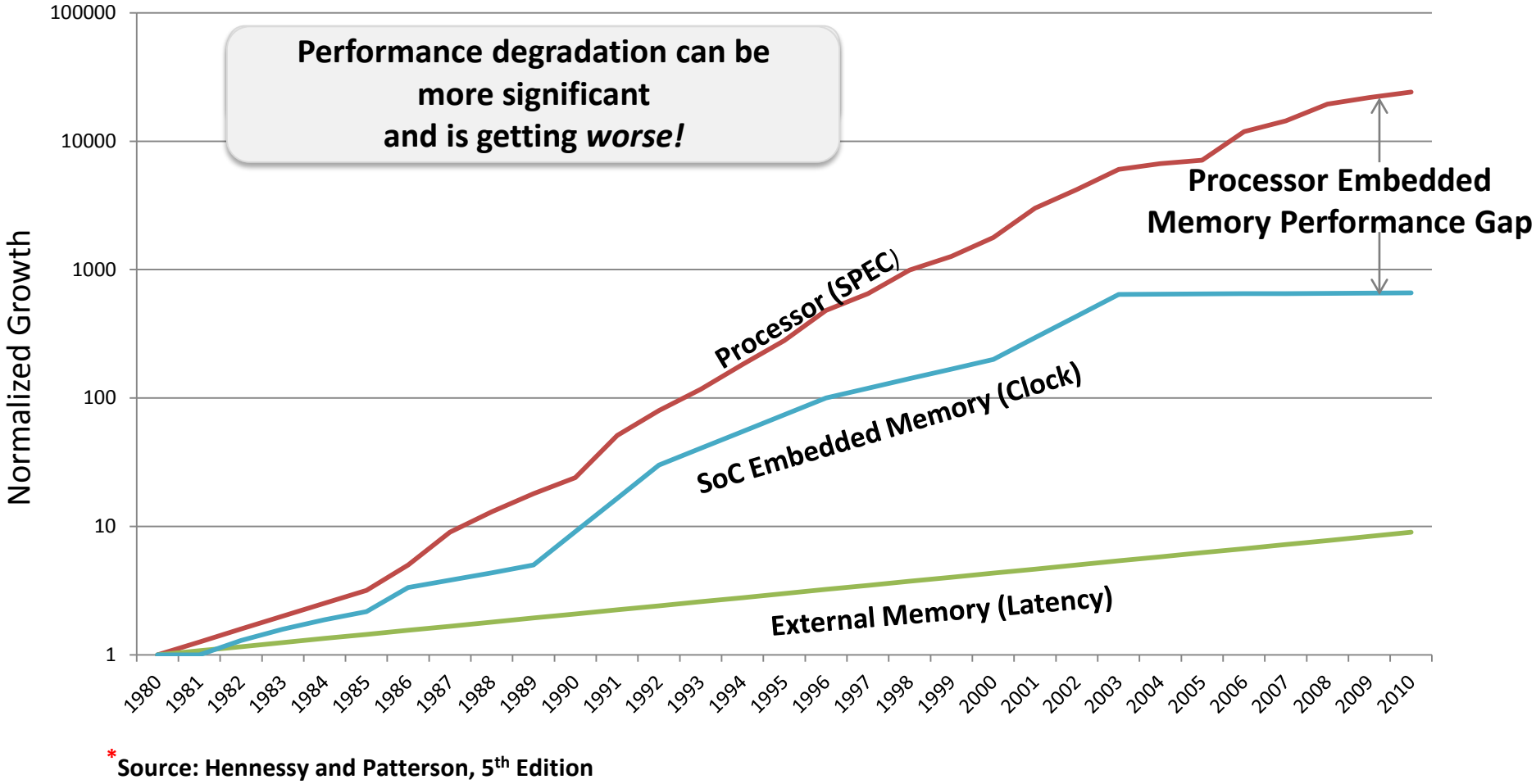
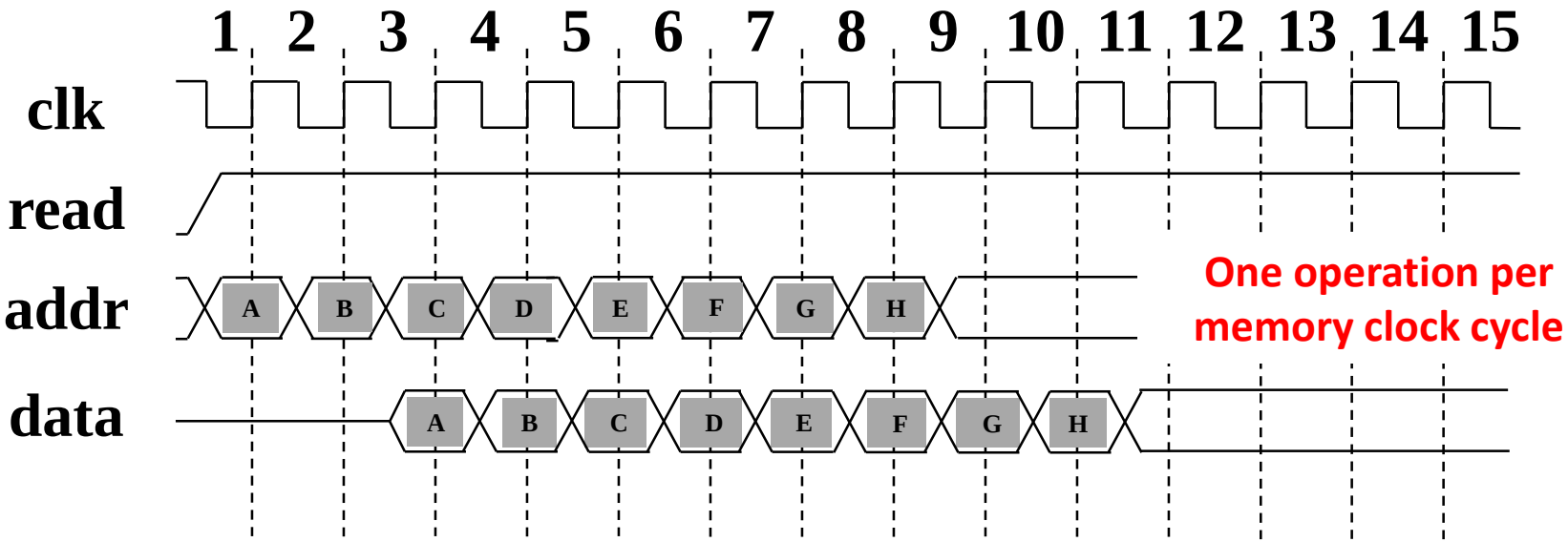
Track F, Lecture 2: Intellectual Property for SoC & Cores

Problem: Processor-Embedded Memory Performance Gap



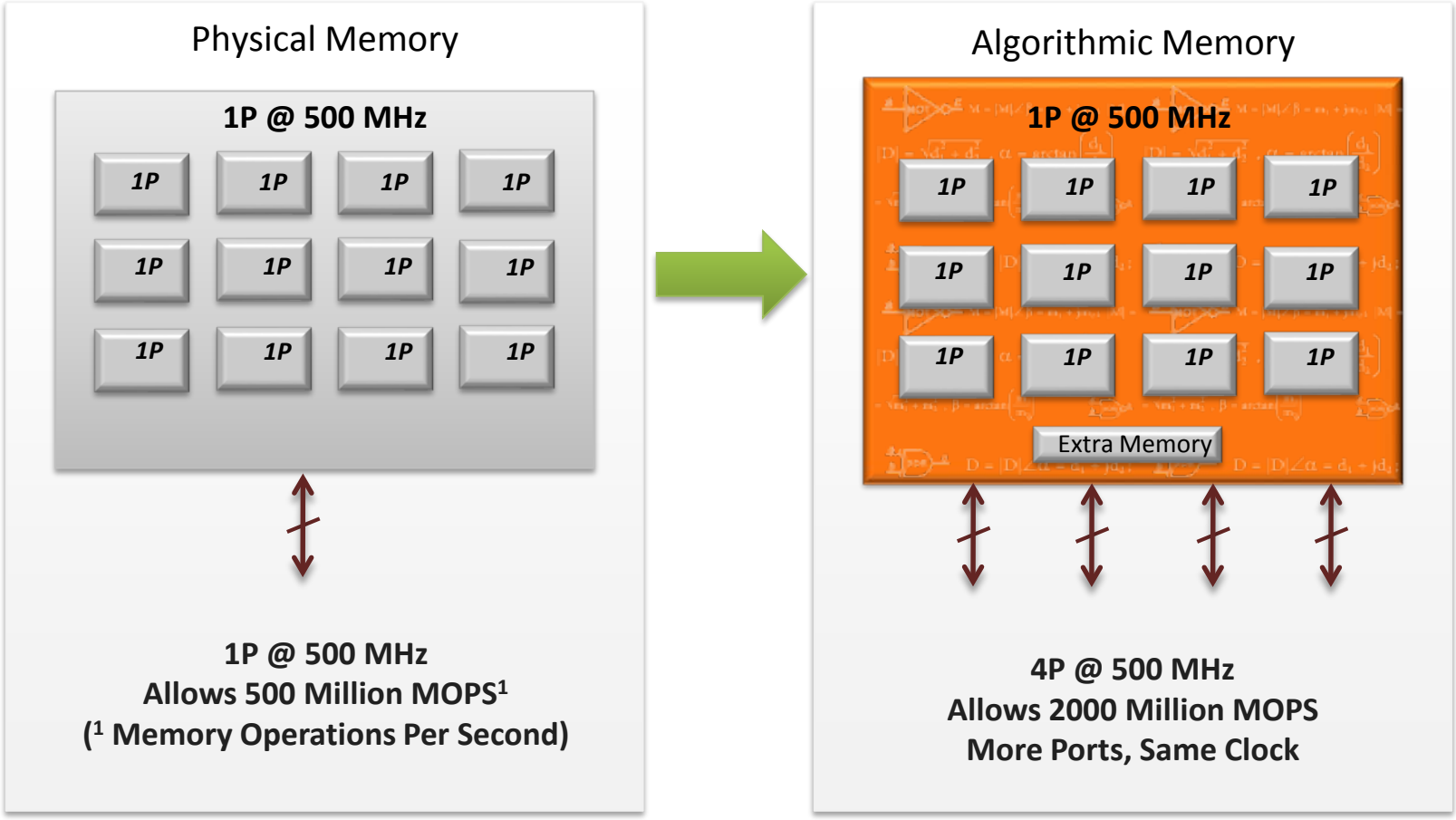
*Source: Hennessy and Patterson, 5th Edition

Why is Embedded Memory Slow?



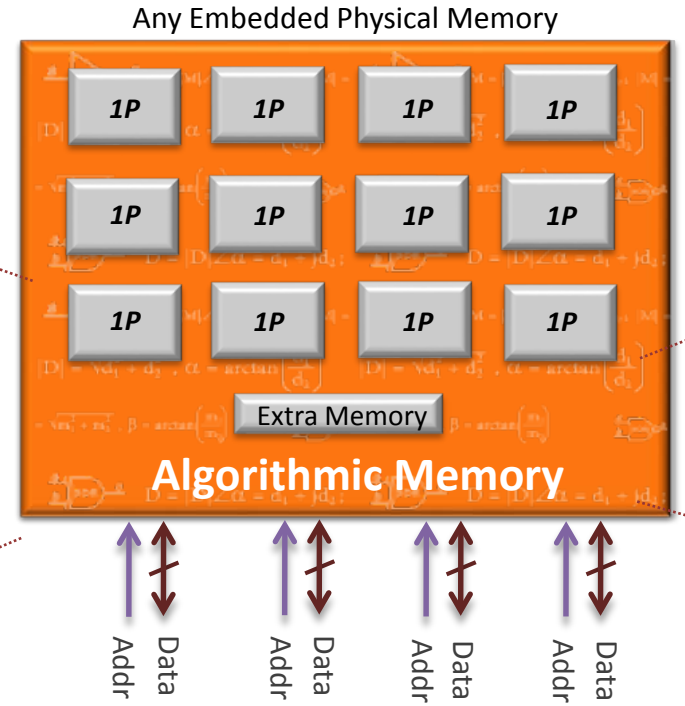
How can we increase memory performance without increasing memory clock speed?

Solution: Algorithmic Memory® = Memory Macros + Algorithms



Solution Overview

2X Performance for ~15% area overhead



RTL Based: No Circuit or Layout changes

Simultaneous Accesses to the same Address, Row, Column, or Bank (no exceptions)

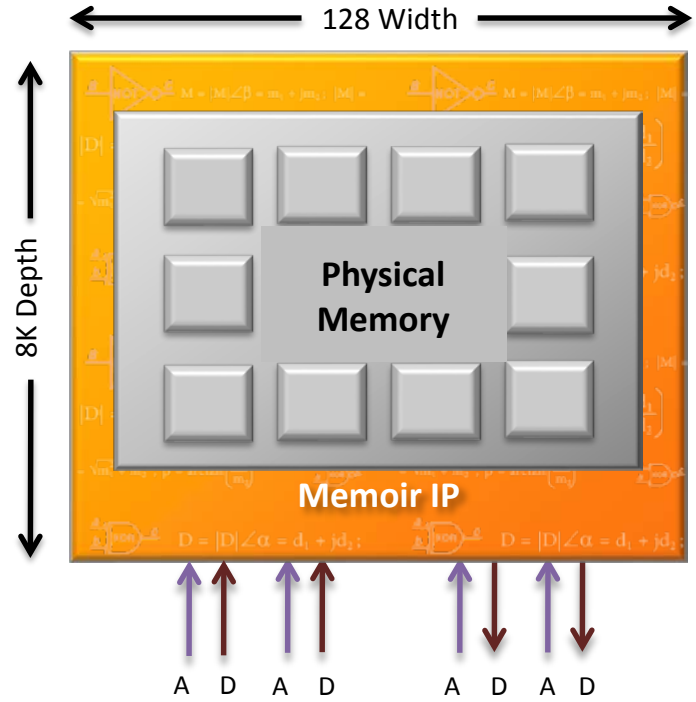
Each Port can access the entire Memory Address

Exhaustively Formally Verified & Transparent to end-user

Using Physical 1-Port Memory to Build any Multiport Functionality

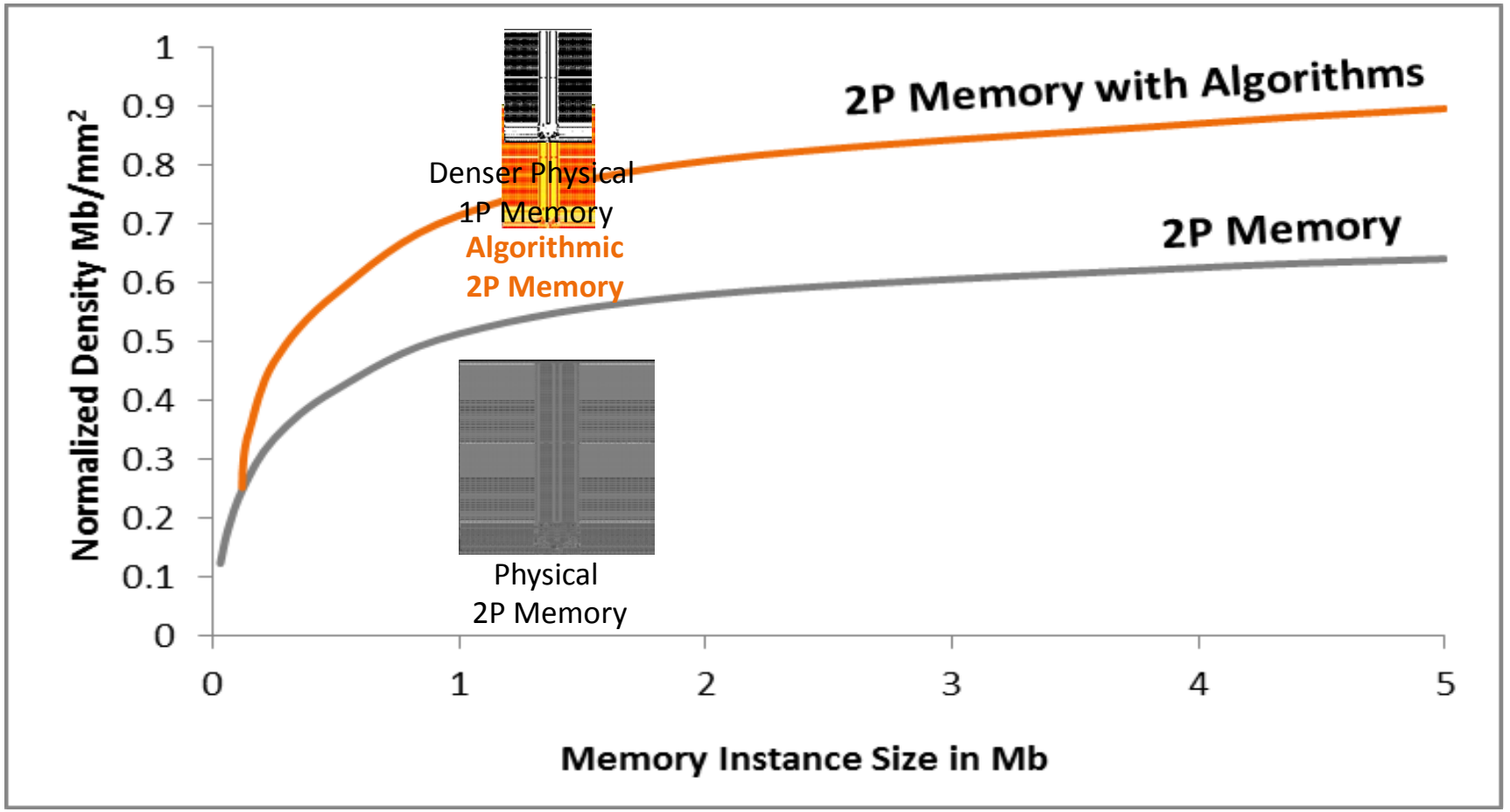
Usage & Adoption

- Easily Interface
  - Presents standard memory interface
  - Adds no clock cycle latency
  - Used as a drop-in replacement
- Readily Integrate
  - Fits seamlessly in SoC design flow
  - Used in SoCs - ASICs, ASSPs, GPPs
- Rapidly Implement
  - Supports any process, node or foundry



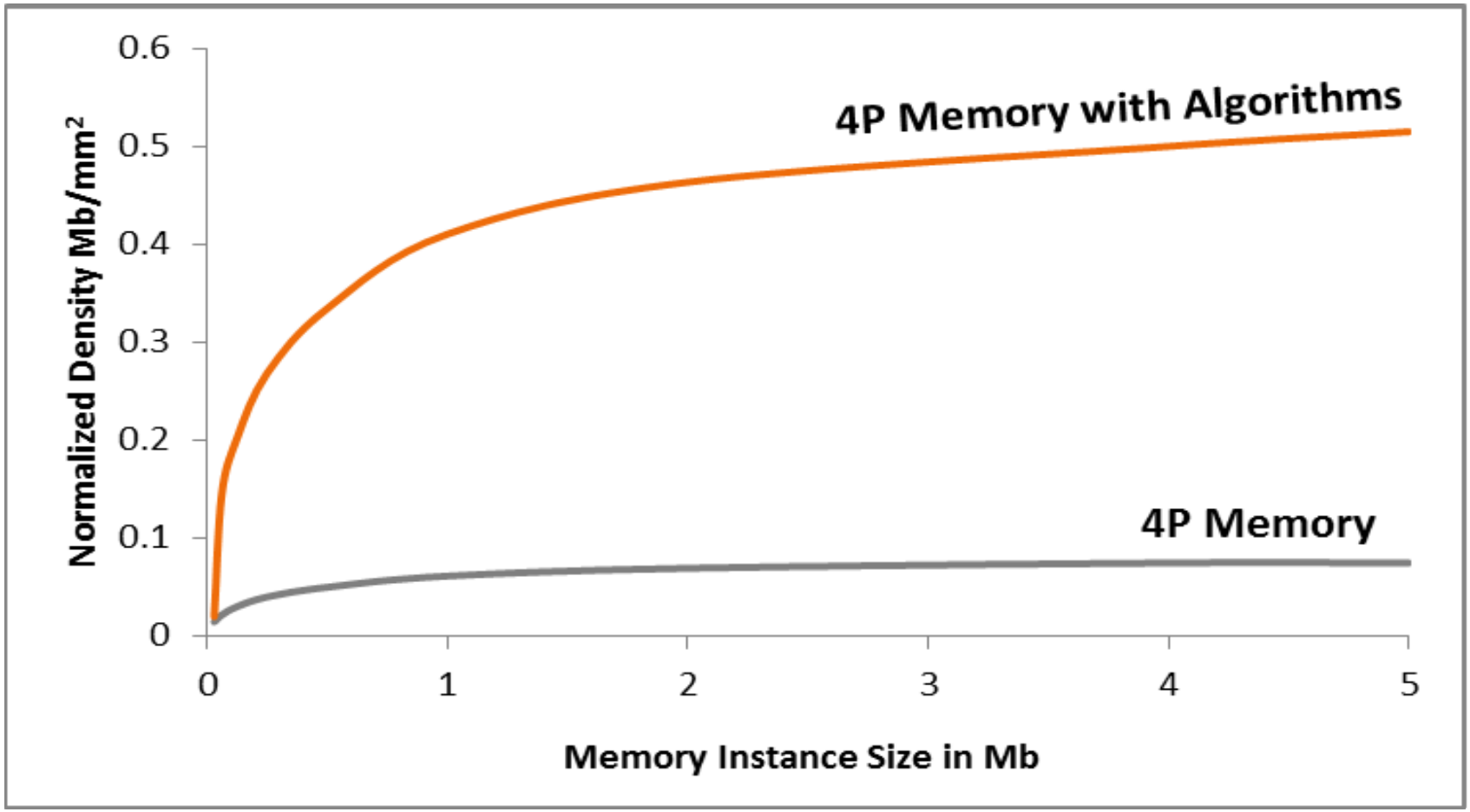
Identical Pinout to Standard Memory

Increases Density



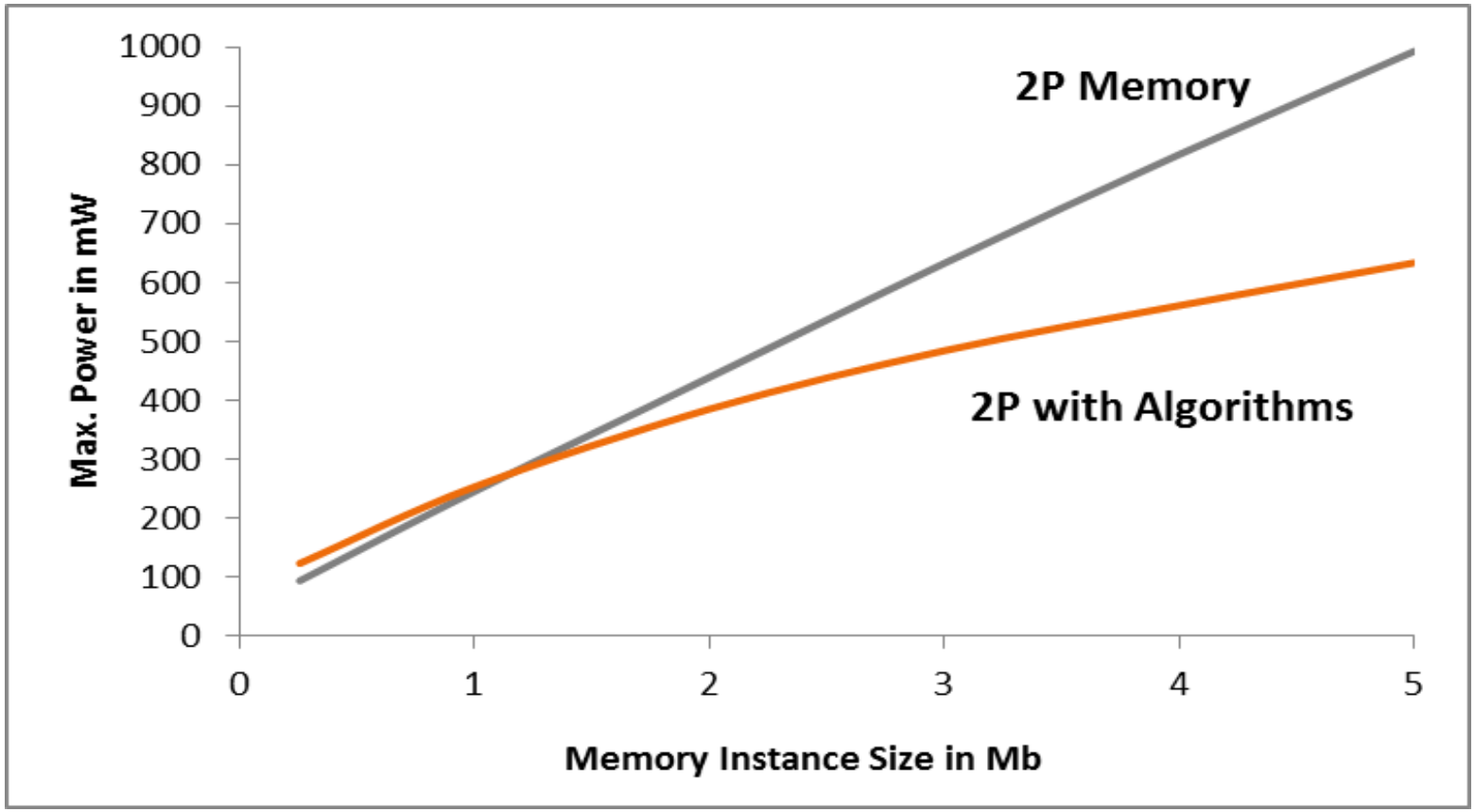
Normalized for 1P = 1 Mb/mm2

Increases Density



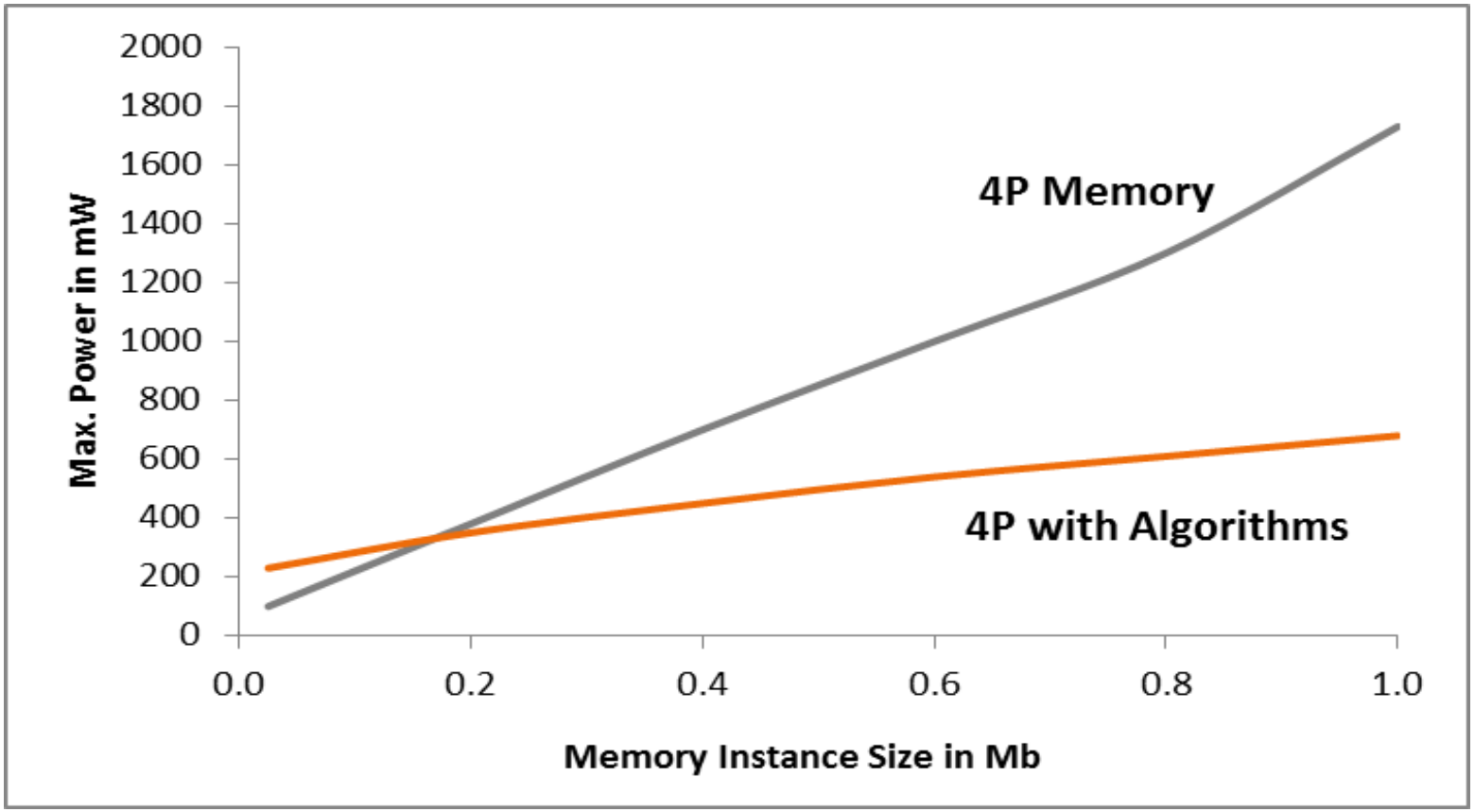
Normalized for 1P = 1 Mb/mm2

Reduces Total Power



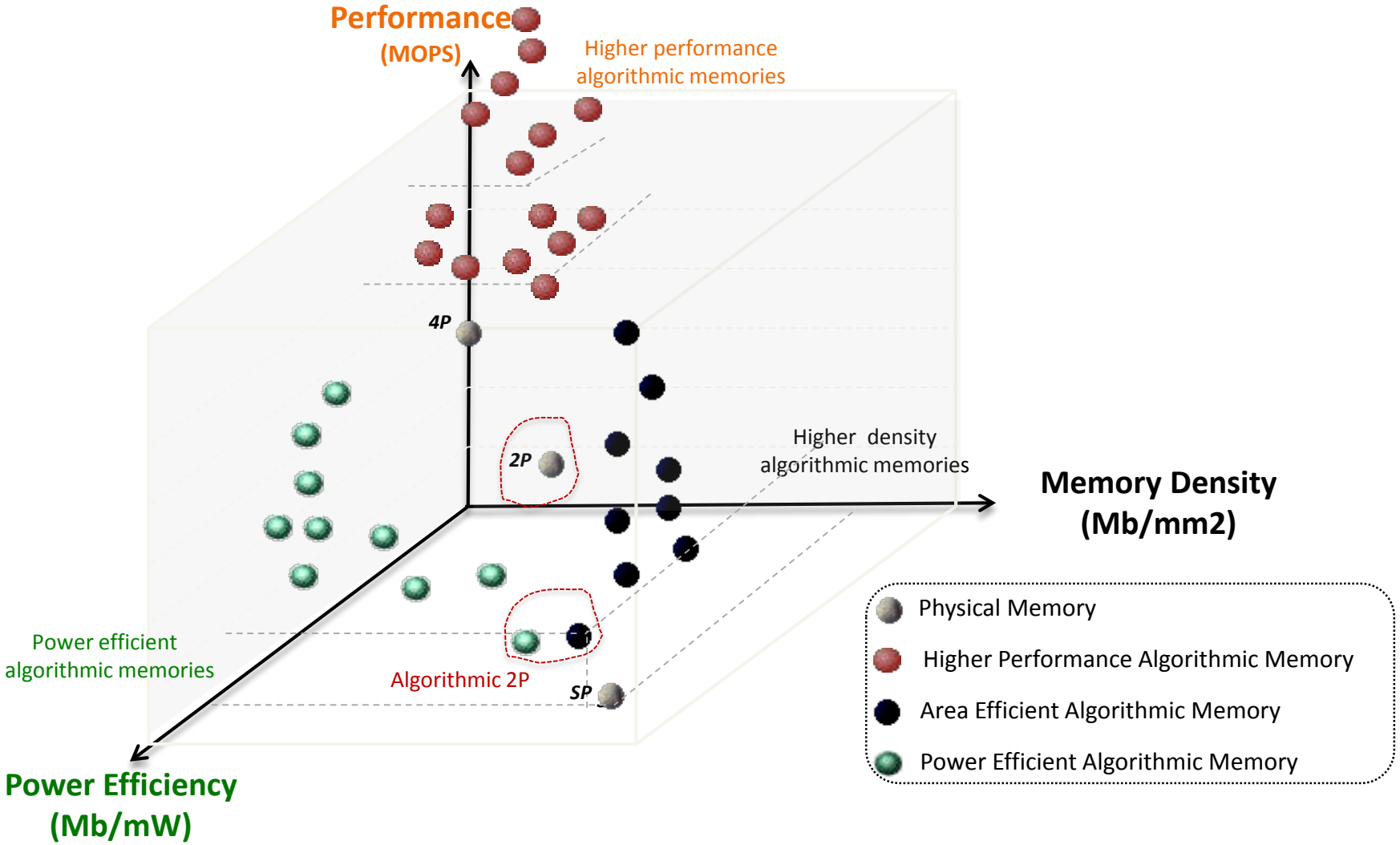
Based on 40nm example

Reduces Total Power

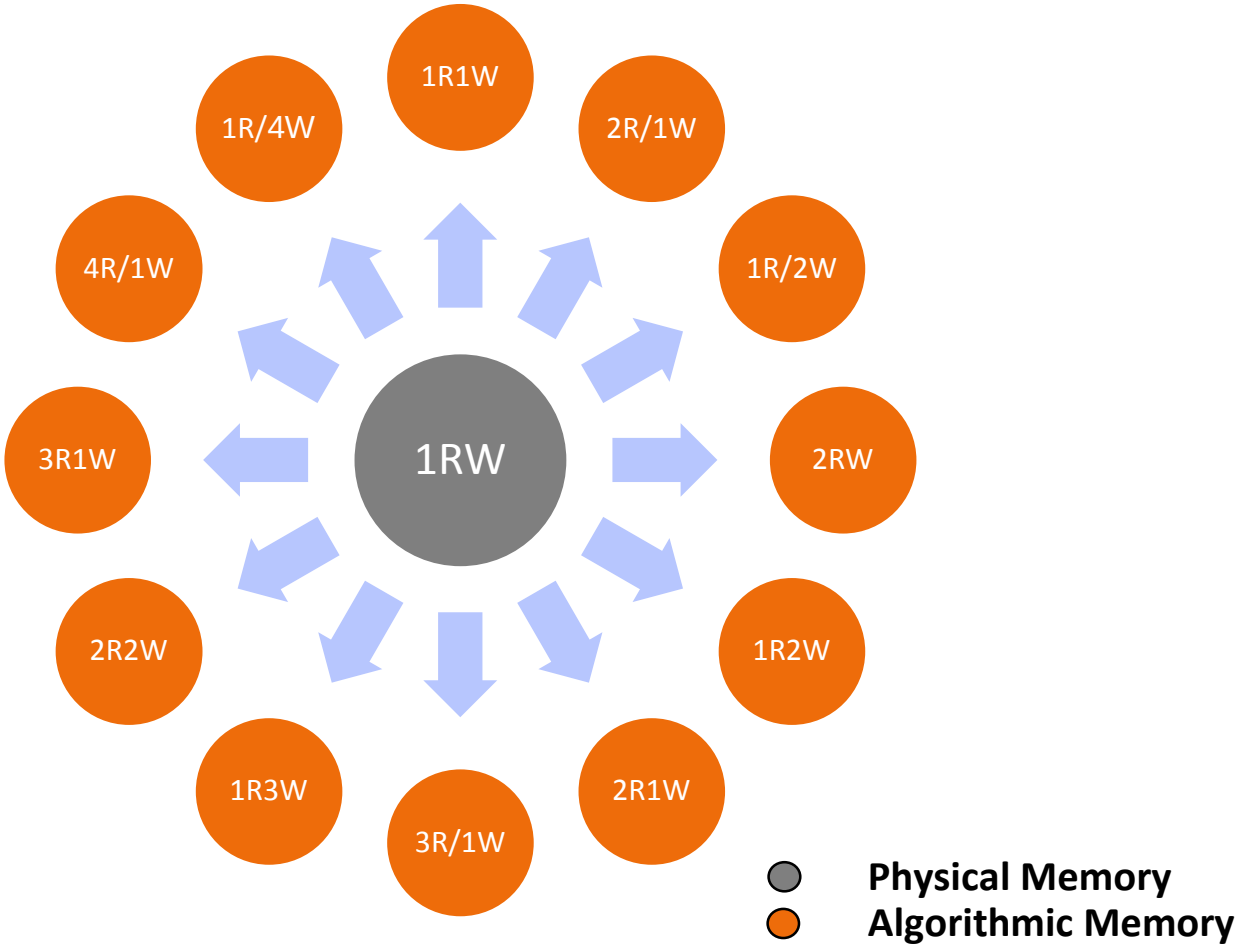


Based on 40nm example

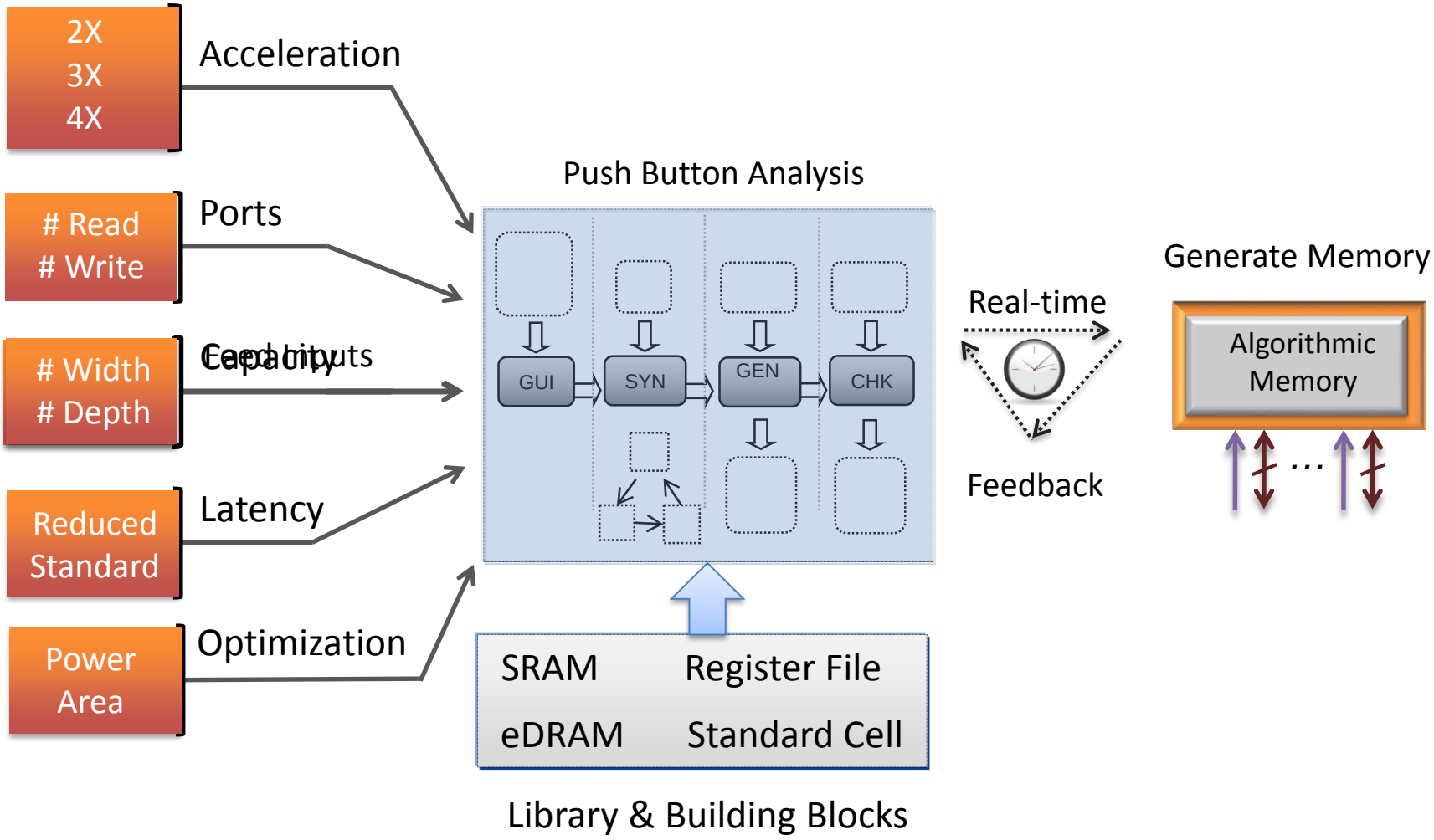
Configurable Performance



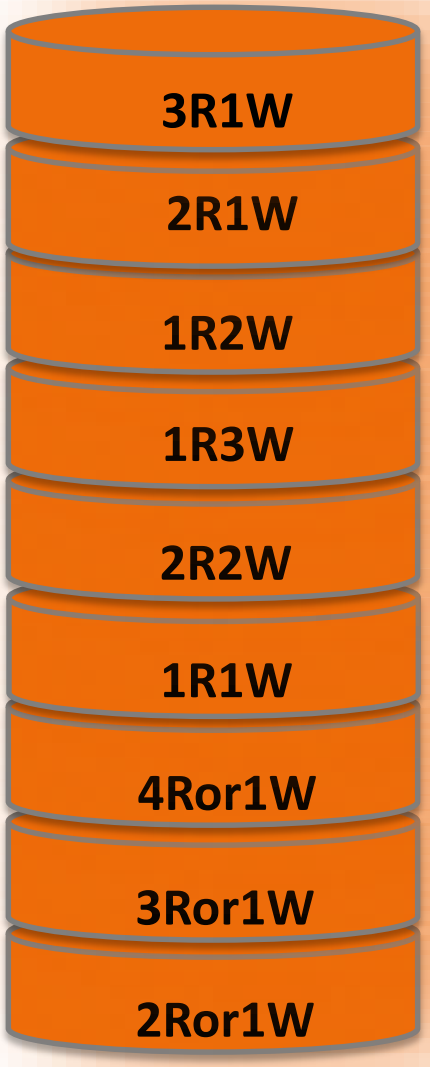
Increases Portfolio of Available Memories



Rapid Memory Analysis & Generation



Multiport Memory Usages



- Descriptor and Free Lists, Ingress Buffers
- L2 MAC Lookups, Shared Caches

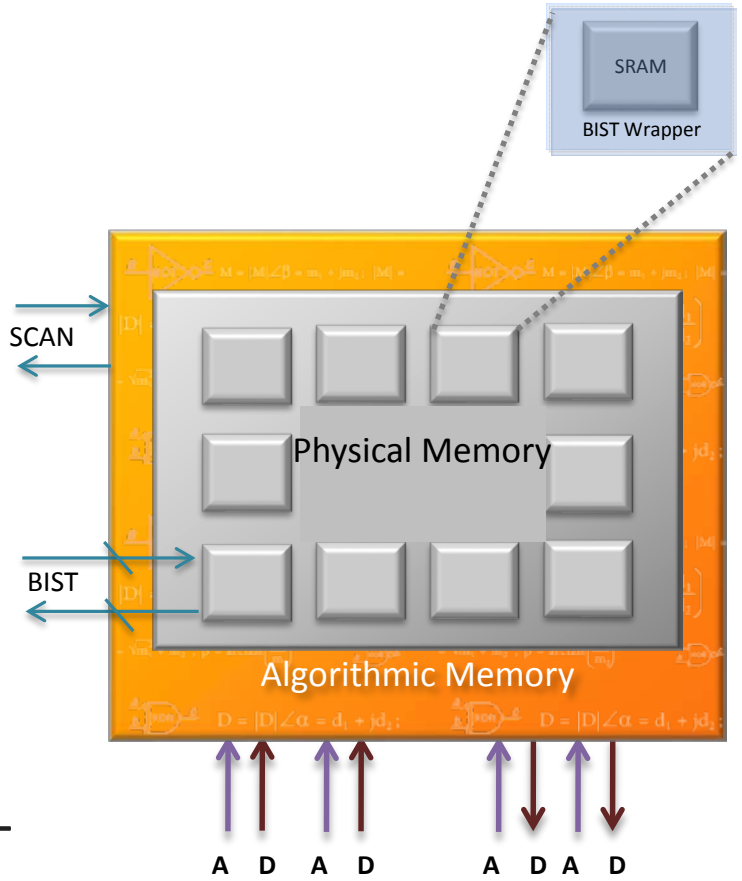
- Descriptor and Free Lists, Egress Buffers
- Cache Coherency Arrays for L2/L3 Caches

- Netflow, Counters
- State Tables, Linked Lists

- Data and Tag Arrays for L2, L3 Caches
- Route Lookup Tables
- ACL Tables

Exhaustive Formal Verification Reduces Risk

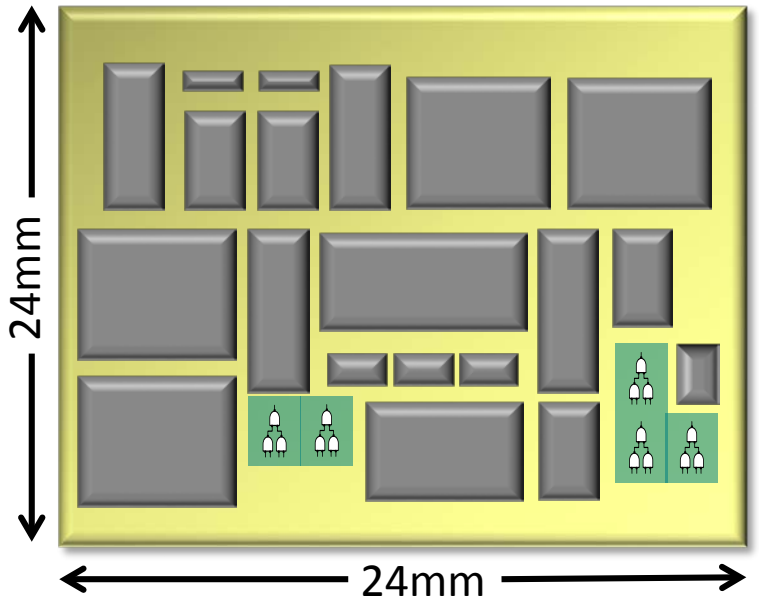
- Independently Verify Logic
  - Mathematically proven algorithms
  - Formally, exhaustively verified RTL
- Separately Test Physical Memories
  - Supports 3rd party DFT methodology
  - Transparent customer BIST, BISR
  - Doesn't need complex multiport BIST



Tier-1 OEM Evaluation

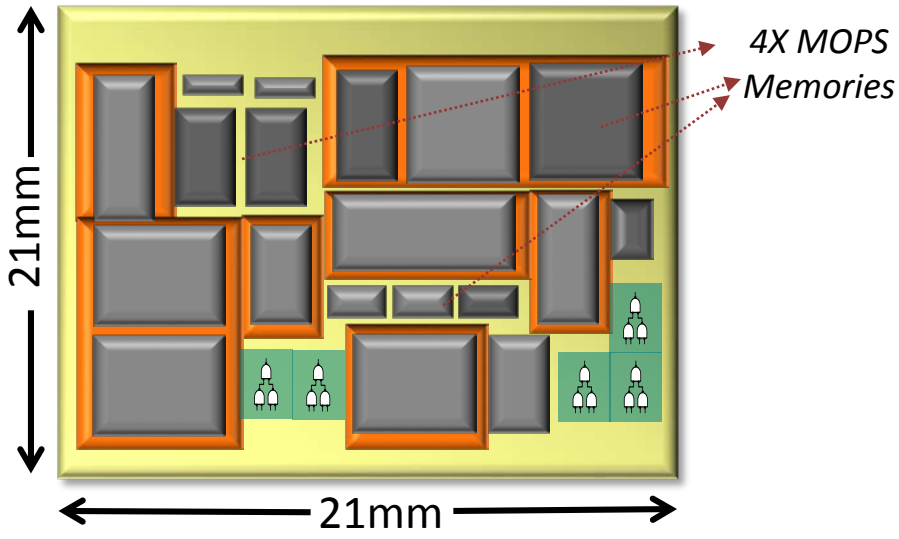
– Performance, Area and Power Benefits

Large ASIC



- Area 576 mm^2
  - 800 Mb of total memory
  - 165 Memory Instances
- Versatile memories required
  - 4R/1W, 2R1W, 1R2W memories

Algorithmic Memory Solution



- Area 441 mm^2
  - Area Savings of 135 mm^2 (23% die)
  - 136 Memory Instances Accelerated
- Power Savings > 12W
- 4X MOPS for select memories

Summary

1. Increases Port and Clock Performance
2. Lowers Area and Power
3. Easy Interface, Integration and Implementation
4. Creates Versatile Memory Portfolio
5. Reduces Cost, Risk and Time to Market

Algorithmic Memories are not a panacea, but present a new solution to alleviate the processor embedded memory performance gap

Q & A

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