Hot Interconnects 15 Tutorial I

Hands-on with the NetFPGA to build a Gigabit-rate Router

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Description

An open platform called the NetFPGA has been developed at Stanford University. The NetFPGA platform enables researchers and instructors to build high-speed, hardware-accelerated networking systems. The platform can be used in the classroom to teach students how to build Ethernet switches and Internet Prototcol (IP) routers using hardware rather than software. The platform can be used by researchers to prototype advanced services for next-generation networks.

By using Field Programmable Gate Arrays (FPGAs), the NetFPGA enables new types of packet routing circuits to be implemented and detailed measurements of network traffic to be obtained. During the tutorial, we will use the NetFPGA to determine the amount of memory needed to buffer TCP/IP data streaming through the Gigabit/second router. Hardware circuits within the NetFPGA will be implemented to measure and plot the occupancy of buffers. Circuits will be downloaded into reconfigurable hardware and tested with live, streaming Internet video traffic.

Outline

* Function of an Internet Router
    - o Control plane
        - + Routing protocols
        - + Routing table
        - + Management and Command Line Interface (CLI)
    - o Datapath
        - + Address lookup
            - # Longest prefix match
            - # Classless Interdomain Routing (CIDR)
        - + Header update
        - + Packet buffer

* NetFPGA Router
    - o Hardware
        - + Gigabit Ethernet interfaces
        - + PCI host interface
        - + Field Programmable Gate Array (FPGA) Logic
        - + Random Access Memory (RAM)
    - o Software
        - + Kernel-space driver
        - + User-space applications
    - o System configuration

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* Demonstration Topology
    - Hardware
        + Network of ten routers
        + Ethernet switch
        + Video server
        + High Definition (HD) video client
    - Software
        + PW-OSPF
        + Routing tables
        + Dynamic re-routing

* Integrated Circuit Design
    - Technologies
        + Look-Up Tables (LUTs)
        + Configurable Logic Blocks (CLBs)
        + Field Programmable Gate Arrays (FPGAs)
    - Verilog Hardware Description Langauge (HDL)
        + Registers, integers, arrays
        + Multiplexers
        + Synchronous storage elements
        + Finite State Machines (FSMs)
    - Hardware Debug
        + Waveform monitor
        + In-circuit logic emulation

* NetFPGA System Components
    - Synthesis of tutorial router
    - Java-based Graphical User Interface (GUI)
        + Configuration
        + Statistics
    - Router architecture
        + Pipeline
        + Queues

* Buffer Size Experiment
    - Experiment with TCP/IP flows
        + Rule-of-thumb for the buffer size
        + Round-trip propation delay
        + Capacity of bottlneck link
        + Number of active flows
    - Lower delay with smaller queues

* Enhanced Router
    - Additional hardware
        + Event capture module
        + Rate limiter
        + Delay module
    - Experiments
        + Netperf
        + HD video transport
    - Life of packet through the system
        + Description of blocks
        + Waveforms from logic analyzer

Bios

Nick McKeown

Nick McKeown is a Professor of Electrical Engineering and Computer Science and Faculty Director of the Clean Slate Program at Stanford University. He received his Phd from the University of California at Berkeley in 1995. From 1986-1989, he worked for Hewlett-Packard Labs in their network and communications research group in Bristol, England. During the Spring of 1995, he worked briefly for Cisco Systems where he helped architect their GSR 12000 router. In 1997 Nick co-founded Abrizio Inc., where he was CTO. Abrizio is now part of PMC-Sierra. He was co-founder and CEO of Nemo Systems, which is now part of Cisco Systems. Nick McKeown is the STMicroelectronics Faculty Scholar, the Robert Noyce Faculty Fellow, a Fellow of the Powell Foundation and the Alfred P. Sloan Foundation, and recipient of a CAREER award from the National Science Foundation. In 2000, he received the IEEE Rice Award for the best paper in communications theory. Nick is a Fellow of the Royal Academy of Engineering (UK), and a Fellow of the IEEE and the ACM, and British Computer Society Lovelace Medal Winner, 2005. He served as an Editor for the *IEEE Transactions on Communications* and *ACM/IEEE Transactions on Networking*, and as a Guest Editor for *IEEE Journal on Selected Areas in Communications, IEEE Networks Magazine* and *IEEE Communications Magazine*, and chaired the Technical Advisory Committee for ACM Sigcomm. Nick's research interests include the architecture of the future Internet, the architecture, analysis and design of high performance switches and Internet routers, IP lookup and classification algorithms, scheduling algorithms, congestion control, routing protocols and network processors.

John W. Lockwood

John W. Lockwood is a Visiting Associate Professor at Stanford University. At Stanford, he is working to develop new applications for the NetFPGA platform. Lockwood's research interests include reconfigurable hardware, Internet security, and content processing technologies. Dr. Lockwood earned his MS, BS, and Ph.D degrees from the Department of Electrical and Computer Engineering at the University of Illinois. Lockwood was granted tenure in the Department of Computer Science and Engineering at Washington University in Saint Louis in 2006. At Washington University in St. Louis, Lockwood led the Reconfigurable Network Group (RNG) to develop the Field programmable Port Extender (FPX) to enable rapid prototype of extensible network modules in Field Programmable Gate Array (FPGA) technology. John Lockwood has served as the principal investigator on grants from the National Science Foundation, Xilinx, Altera, Nortel Networks, Rockwell Collins, and Boeing. He has worked in industry for AT&T Bell Laboratories, IBM, Science Applications International Corporation (SAIC), and the National Center for Supercomputing Applications (NCSA). He served as a co-founder of Global Velocity, a networking startup company focused on high-speed data security. He is a member of IEEE, ACM, Tau Beta Pi, and Eta Kappa Nu.

Jad Naous

Jad is a PhD student at Stanford University. He earned his Master of Science in Electrical Engineering from Stanford in 2007 and his Bachelor of Engineering in Computer Engineering from McGill University in 2005. He has been working on the NetFPGA since 2006, and has recently developed the base router and switch designs on the NetFPGA as well as a high precision event capture system for monitoring queue occupancies.

Glen Gibb

Glen is a PhD candidate in Electrical Engineering at Stanford University. He received his Master of Science in Electrical Engineering from Stanford University and a Bachelor of Science and a Bachelor of Engineering from The University of Melbourne in Australia. He has been working on the NetFPGA platform since 2004 and was the lead designer for the current hardware version.

Adam Covington

Adam Covington is a member of research staff at Washington University. Upon completing his BS degree in Computer Engineering in 2003, Adam earned his MS degree in Computer Science and Engineering at Washington University in December of 2006. At Stanford, Adam has helped to assemble the NetFPGA test systems.