AN OVERVIEW OF HARDWARE ISSUES
FOR IP AND ATM

"Name one thing you could achieve with ATM that you couldn't with IP!"

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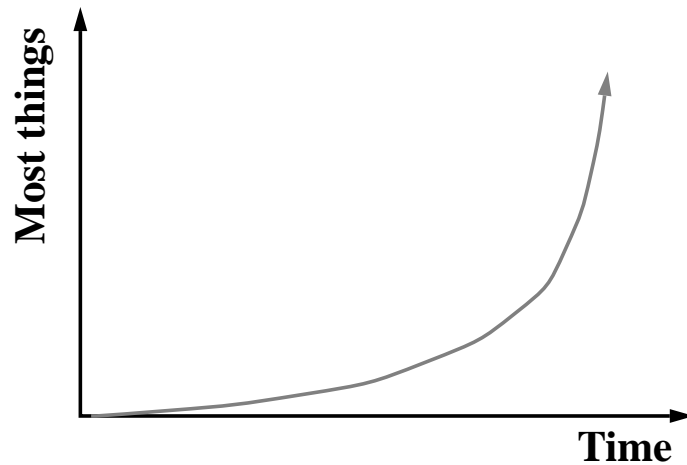http://ee.stanford.edu/~nickm**

Outline

Part I

- **The need**
- **Trends in ATM switches**
- **Trends in IP routers**
- **Merging of the two**

Part II

- **Some key technologies**
- **Summary**

What's the Problem?

Most things vs Time

The demand
The San Jose NAP

Aggregate bandwidth (Mbps) — Feb 100, Apr 123, Jun 150, Aug 200, Nov 460

Source: http://www.mfsdatanet.com/MAE/west.stats.html

The supply

Router Performance (packets/second)

10^5

10^4

10^3

1986   1990   1994
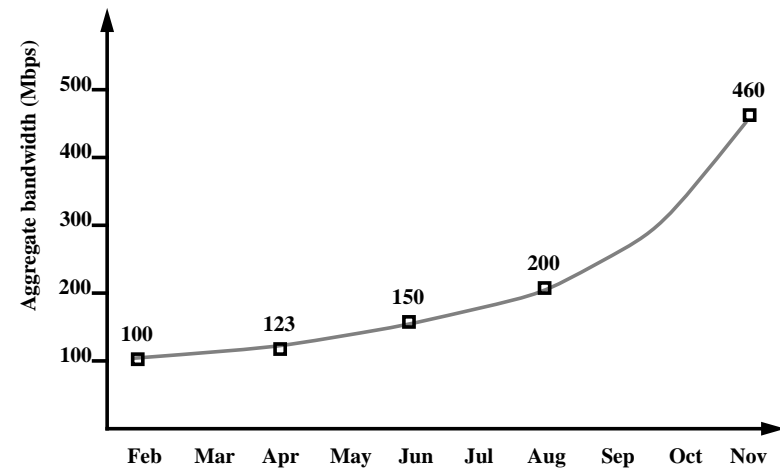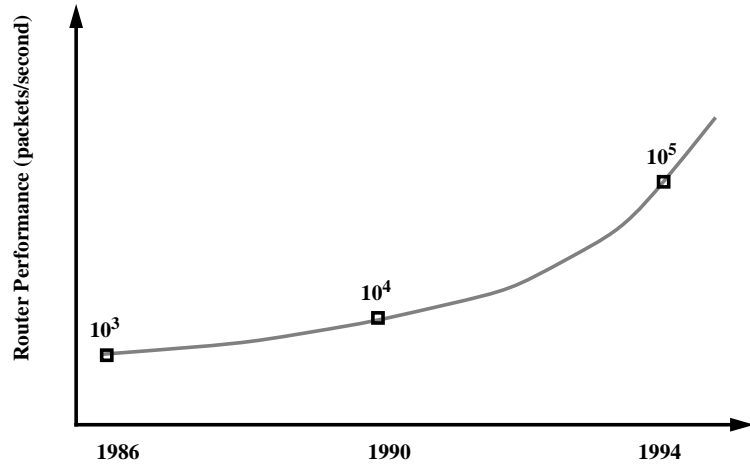
Why we need faster routers

packets/second

Demand

Supply

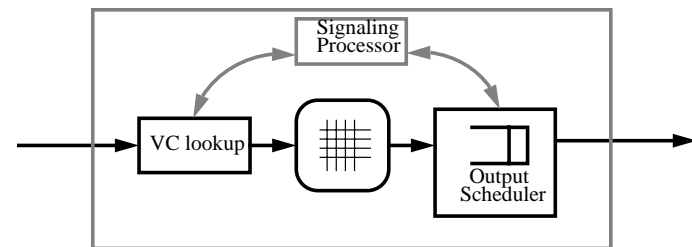1986   1990   1994

The race is on...

packets/second

Demand

Supply
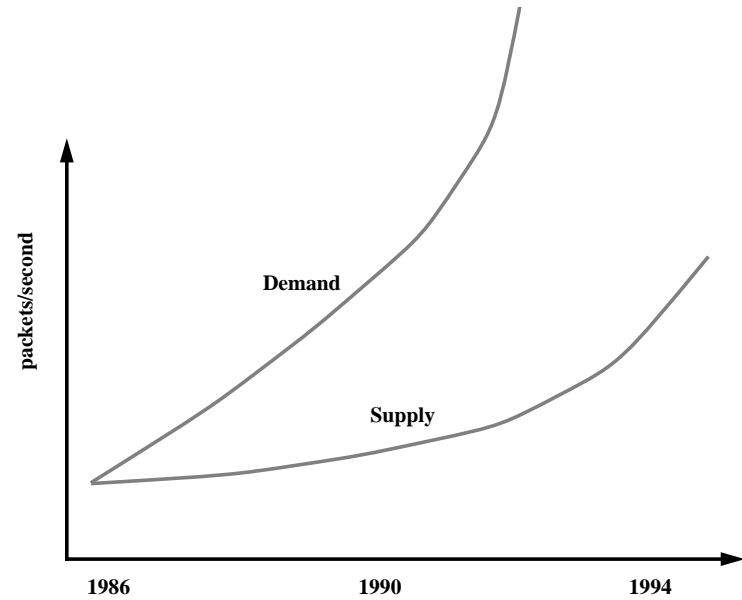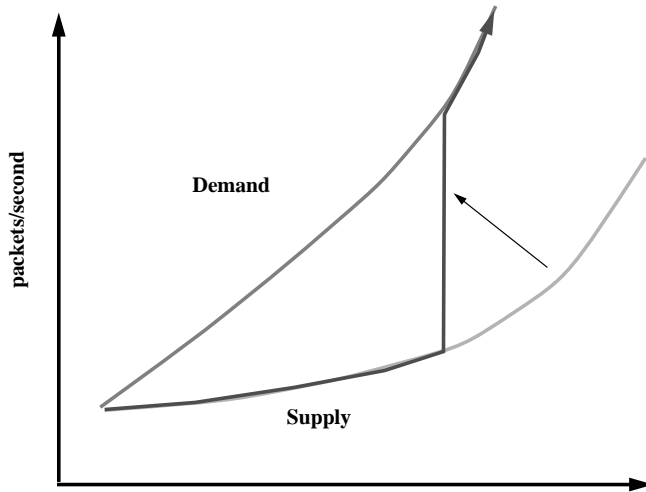
Ascend (Netstar), Ipsilon, Toshiba, BBN, [Cisco, Bay, Juniper, Torrent] ?........

Trends in ATM switches

Generic ATM Switch:

Signaling Processor

VC lookup

Output Scheduler

Trends in IP routers

Generic IP Router:
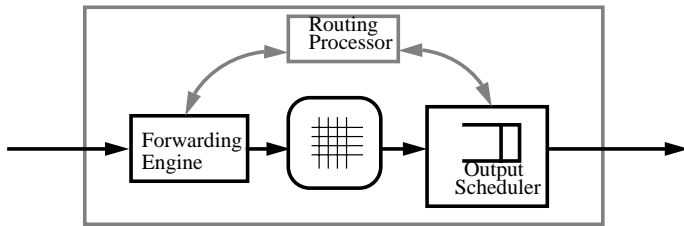
Merging of IP & ATM

- Copy rate
- Arrival rate
- Header processing time
- Min back-to-back packet size
- **Packet size**

Merging of IP & ATM

- **Most routers do this poorly!**
- Copy rate
- Arrival rate
- Header processing time
- Min back-to-back packet size
- **Packet size**
- **Most routers today use caching**
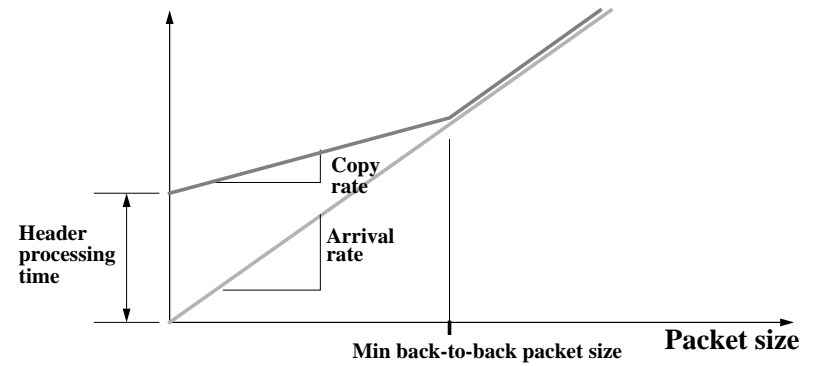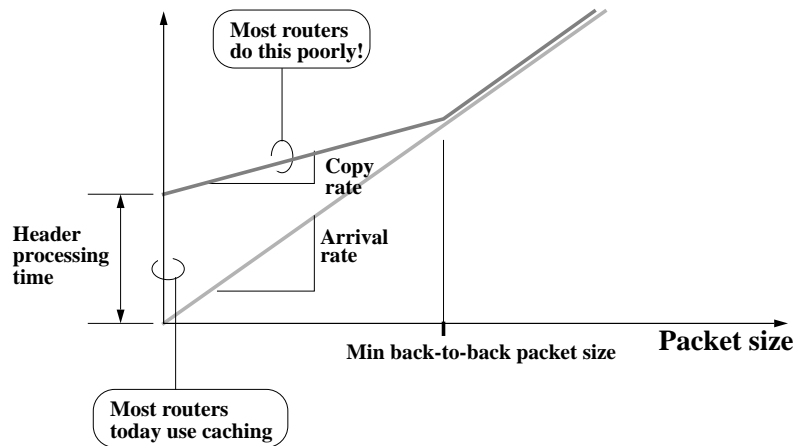
Trends in IP routers
Trend 1: Move CPU off forwarding path

① CPU

② CPU
HW CACHE
HW CACHE
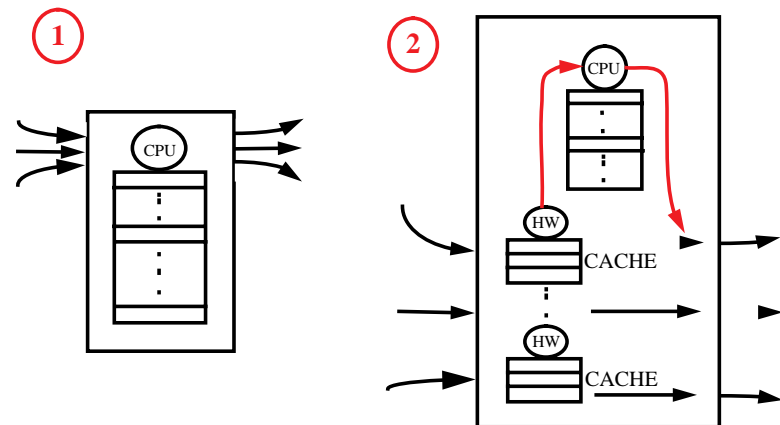
Trends in IP routers
Trend 2: *AVOID SHARED BUS*

① ②

LINE

CPU

LINE

Consequence

① Ⓐ

ROUTER

VCXT   VCXT

VCXT   VCXT

TAG TABLE

TAG TABLE

IP Switching   **Tag Switching**
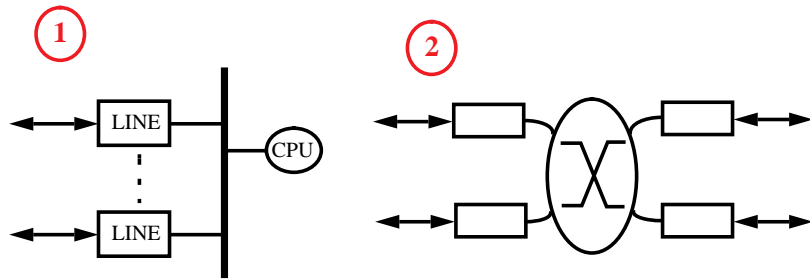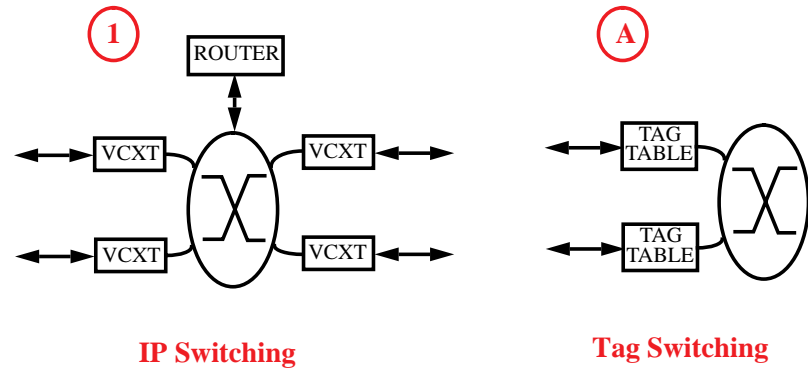
The fundamental hardware difference between IP & ATM

24

VCI → VCXT →

1 ENTRY PER ACTIVE FLOW

32-64K

32

IP DA → FWD TABLE →

1 ENTRY PER DEST. SUBNET

50-100K
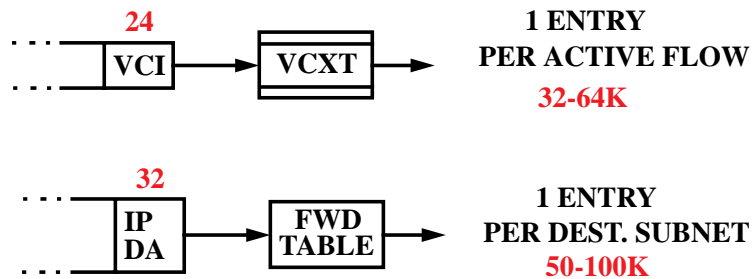
BUT:

   ATM VCI $\cong$ 16 bits AND we get to choose!

Claim

If we could do FAST longest prefix matches

Then we wouldn't be here!

Merging of IP & ATM
Why?

If you could get the whole IP forwarding table in fast memory (and update it invisibly!) then who needs ATM?

Removing IP forwarding engine from the datapath is one thing: but still need Quality Processor on the critical path.

Large number of individual flows (ISMP Flow Type 1)
=> aggregation onto coarser src-dest flows (Type 2)
=> need reassembly/frame-mode switches

Some key hardware technologies
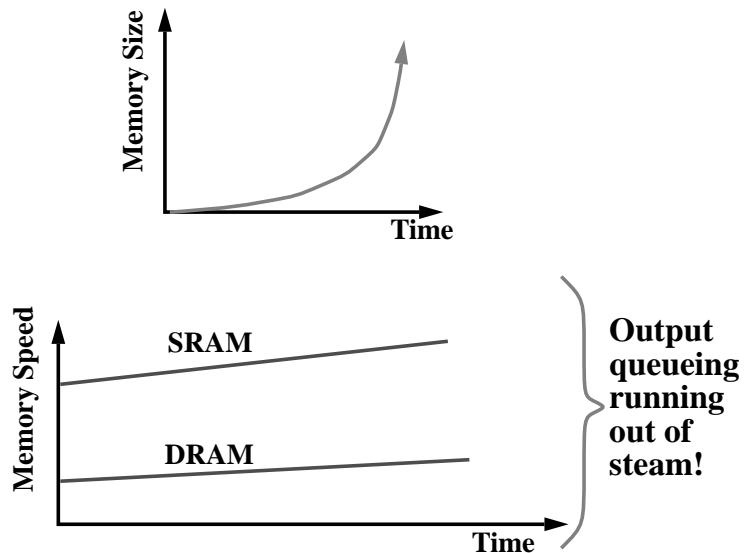
- **Memory bandwidth**
- **Serial link technology**

- **Special-purpose memories**
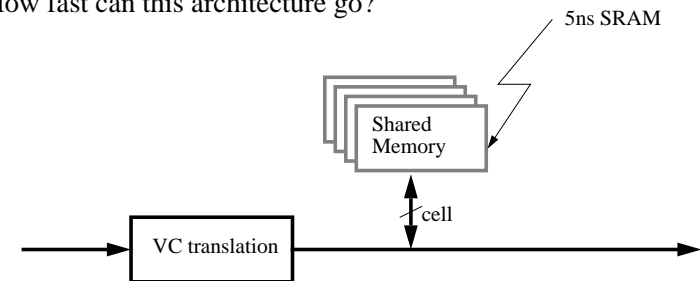- **CPU vs special-purpose processors**

Memory Bandwidth

Output queueing running out of steam!
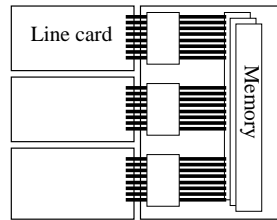
Trends in ATM switches

How fast can this architecture go?

How fast can a 16 port switch operate with this architecture?

· cell per port

Serial link technology

"wires are becoming a scarce resource"

Line card | Memory

Standard interfaces are a bottleneck:

- **100 Mbit/sec per pin is tough.**
- **100 signal pins for 10 Gbit/sec.**
- **Large chip packages and board connectors drive up costs.**

Serial interfaces are efficient:

- **1 Gbit/sec per pin.**
- **10 signal pins for 10 Gbit/sec.**

Serial link technology

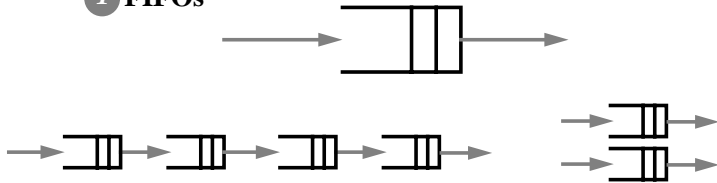## *Problems with High Speed Links*

- **Precise timing needed**
  - — **Hard to determine which bit is which.**
  - — **Distributed clocks have skew (1 ns/bit time at 1 Gb/s).**
  - — **Solution: recover timing from data.**

- **High speed signals**
  - — **Need to transmit and receive 1 Gb/s.**
  - — **Solutions: low swing signals, good terminations on transmission lines.**
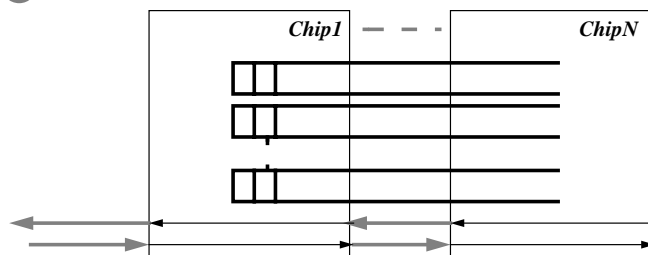
Much ongoing R&D in this area.
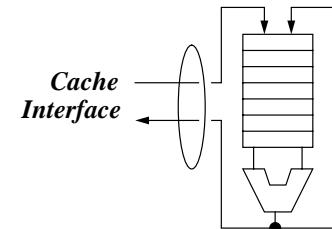

Special purpose memories

1 FIFOs

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2 Programmable FIFOs

Chip1 — — — *ChipN*

CPU vs. special-purpose processor

1

Cache Interface

2

Packets

Data

Data copy

Header

Packets

Forwarding Tables   **e.g. BayBridge**
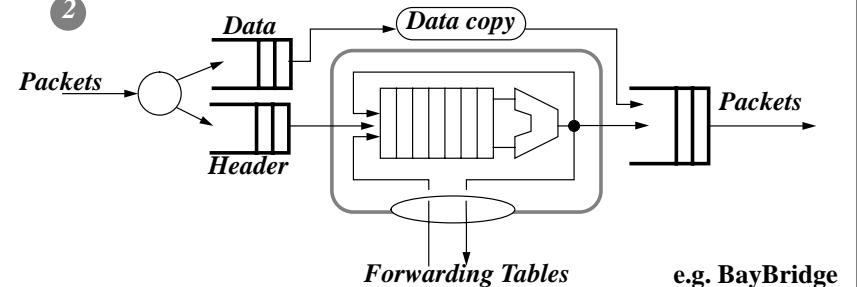
Summary

- **Trends in switching**
  — **Single-stage shared memory and busses are running out of steam.**
  — **Combined I/O Queueing and/or multistage switches are require.**

- **Trends in routing**
  — **Removal of CPUs from forwarding path.**
  — **Quality Processor still on the main forwarding path.**

- **Key Technologies**
  — **Memory Bandwidth**
  — **Serial link technology**
  — **Special-purpose memory**
  — **Special-purpose processors**