Algorithmic Memory Increases Memory Performance By an Order of Magnitude

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Track F, Lecture 2: Intellectual Property for SoC & Cores
Problem: Processor-Embedded Memory Performance Gap

Performance degradation can be more significant and is getting worse!

*Source: Hennessy and Patterson, 5th Edition
Why is Embedded Memory Slow?

One operation per memory clock cycle

How can we increase memory performance without increasing memory clock speed?
Solution: Algorithmic Memory® = Memory Macros + Algorithms

Physical Memory

1P @ 500 MHz

1P  1P  1P  1P
1P  1P  1P  1P
1P  1P  1P  1P

1P @ 500 MHz
Allows 500 Million MOPS
(1 Memory Operations Per Second)

Algorithmic Memory

1P @ 500 MHz

4P @ 500 MHz
Extra Memory

1P  1P  1P  1P
1P  1P  1P  1P
1P  1P  1P  1P

4P @ 500 MHz
Allows 2000 Million MOPS
More Ports, Same Clock
Solution Overview

Using Physical 1-Port Memory to Build any Multiport Functionality

2X Performance for ~15% area overhead

RTL Based: No Circuit or Layout changes

Each Port can access the entire Memory Address

Any Embedded Physical Memory

Simultaneous Accesses to the same Address, Row, Column, or Bank (no exceptions)

Exhaustively Formally Verified & Transparent to end-user

Using Physical 1-Port Memory to Build any Multiport Functionality

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Usage & Adoption

- **Easily Interface**
  - Presents standard memory interface
  - Adds no clock cycle latency
  - Used as a drop-in replacement

- **Readily Integrate**
  - Fits seamlessly in SoC design flow
  - Used in SoCs - ASICs, ASSPs, GPPs

- **Rapidly Implement**
  - Supports any process, node or foundry

Identical Pinout to Standard Memory

Physical Memory

8K Depth

128 Width

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Increases Density

Normalized for $1P = 1 \text{Mb/mm}^2$

Denser Physical
1P Memory
Algorithmic
2P Memory

Physical
2P Memory

Normalized for $1P = 1 \text{Mb/mm}^2$
Increases Density

4P Memory with Algorithms

4P Memory

Normalized Density Mb/mm²

Memory Instance Size in Mb

Normalized for 1P = 1 Mb/mm²
Reduces Total Power

Based on 40nm example
Reduces Total Power

Based on 40nm example
Configurable Performance

Performance (MOPS)

Memory Density (Mb/mm²)

Power Efficiency (Mb/mW)

Higher performance algorithmic memories

Higher density algorithmic memories

Algorithmic 2P

Physical Memory

Higher Performance Algorithmic Memory

Area Efficient Algorithmic Memory

Power Efficient Algorithmic Memory
Increases Portfolio of Available Memories

Algorithmic Memory

Physical Memory

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Rapid Memory Analysis & Generation

- 2X
- 3X
- 4X

- Acceleration
- Ports
- # Read
- # Write
- # Width
- # Depth
- Capacity
- Latency
- Reduced
- Standard
- Optimization
- Power
- Area

Push Button Analysis

SRAM
Register File

eDRAM
Standard Cell

Library & Building Blocks

Real-time
Feedback

Generate Memory

Algorithmic Memory

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Multiport Memory Usages

- Descriptor and Free Lists, Ingress Buffers
- L2 MAC Lookups, Shared Caches
- Netflow, Counters
- State Tables, Linked Lists
- Data and Tag Arrays for L2, L3 Caches
- Route Lookup Tables
- ACL Tables

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Exhaustive Formal Verification Reduces Risk

- Independently Verify Logic
  - Mathematically proven algorithms
  - Formally, exhaustively verified RTL

- Separately Test Physical Memories
  - Supports 3\textsuperscript{rd} party DFT methodology
  - Transparent customer BIST, BISR
  - Doesn’t need complex multiport BIST
Tier-1 OEM Evaluation
— Performance, Area and Power Benefits

Large ASIC

- Area 576 mm²
  - 800 Mb of total memory
  - 165 Memory Instances
- Versatile memories required
  - 4R/1W, 2R1W, 1R2W memories

Algorithmic Memory Solution

- Area 441 mm²
  - Area Savings of 135 mm² (23% die)
  - 136 Memory Instances Accelerated
- Power Savings > 12W
- 4X MOPS for select memories

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Summary

1. Increases Port and Clock Performance
2. Lowers Area and Power
3. Easy Interface, Integration and Implementation
4. Creates Versatile Memory Portfolio
5. Reduces Cost, Risk and Time to Market

Algorithmic Memories are not a panacea, but present a new solution to alleviate the processor embedded memory performance gap
Q & A

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