SUNDAR IYER

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PARTICULARS

EDUCATION

Stanford University — Stanford, CA
Ph. D. in Computer Science[†] — *July 2008*
Thesis: Load Balancing and Parallelism for the Internet

Stanford University — Stanford, CA
M. S. in Computer Science — *June 2000*
Distinction in Research

Indian Institute of Technology (I. I. T.), Bombay — Mumbai, India
B. Tech. in Computer Science and Engineering — *April 1998*

ENTREPRENEURSHIP

- **Co-Founder, CEO, and Member of the Board, Memoir Systems,** Mar 2009 - Current, CTO from July 2011 - Dec 2012. Memoir Systems is a fabless semiconductor IP company building Algorithmic Memory technology to solve the ever increasing 'processor-embedded memory' performance gap. Memoir's standard and custom products increase embedded memory performance by 4X, and up to 10X respectively. The performance guarantee is mathematically proven, and exhaustively formally verified. Current usages include high-performance networking, cloud infrastructure, data-center, storage networking, software-defined networking, and HD-video applications. Other applications such as mobile and multicore processing, including high-end applications such as supercomputing, genome sequencing, weather simulations all benefit from significantly higher memory performance. Memoir's Algorithmic Memory technology is the recipient of several awards, and is currently adopted by multiple customers including tier-1 OEMs, tier-1 ASSP vendors, tier-1 ASIC vendors, and by top-5 semiconductor manufacturers.
- **Co-Founder, CTO, and Member of the Board, Nemo Systems,** Nov 2003 - Sep 2005. Nemo Systems (acquired by Cisco Systems in Sep 2005) was a fabless semiconductor IP company, building 100% hit-rate caching algorithms for scaling the performance of high-speed networking memory systems beyond 100Gb/s, based on the mathematical work done during my Ph.D. thesis at Stanford University. The technology reduced the cost of router SRAMs, by over a hundred million dollars. It allowed routers to guarantee deterministic memory performance, make them more robust against performance based denial of service attacks, and give better deterministic latency guarantees for critical real-time applications on the Internet.
- **Founding Member, and Senior Systems Architect, SwitchOn Networks,** Jan. 1999 - Sep. 2000. SwitchOn Networks (acquired by PMC-Sierra in Sep. 2000) was a fabless semiconductor company building a co-processor for high-performance data communication systems. The company's technology was developed in collaboration with IIT Bombay, and the company was one of the pioneers in content and deep packet processing, enabling key applications such as application based security, virus filtering, and server load balancing in the early days of the Internet. The company's customers included tier-1 networking OEMs, and leading service providers.

WORK EXPERIENCE

- **Technical Leader, Co-lead Network Memory Group, Cisco Systems,** Oct 2005 - Dec 2008. The Network Memory Group focussed on the deployment of the memory caching technology developed at Nemo Systems, and new development of memory intelligence and I/O serialization technology. The group developed architectural solutions, and developed multiple generations of network memory ASICs, used across Cisco's

[†]On leave of absence from March 2003 to March 2008.

high-speed enterprise and core switching products. The technology was fast-tracked by Cisco's central development organization in August 2007, to be proliferated widely across the campus, core, and enterprise infrastructure. The technology and products were integrated in over 15 unique instances, on more than 7 unique Cisco platforms, helping scale networking performance to 400Gb/s and beyond.

- **Consultant, Nevis Networks Inc.**, Sep. 2003 - Mar 2004. Developed theoretically optimal and practical packet switching algorithms to achieve 100% throughput, for the distributed shared memory switch fabric.
- **Systems Engineer, PMC-Sierra,** Sep. 2000 - Oct. 2001. Jointly developed architecture and algorithms for a second generation content and deep packet classification co-processor, ClassiPI.

AWARDS & HONORS

1. IIT Bombay, Young Alumni Achiever Award, March 2014.
2. As Part of Memoir Systems —
   - Gartner Cool Vendor, March 2014.
   - EE-Times Top 10 Memory Design Features for Algorithmic Memory Technology, Dec. 2012.
   - EE Times 60 Emerging Silicon Startups for Memoir Systems, Oct. 2012.
   - Red Herring Top 100 Award for Memoir Systems, May 2012.
   - Selected Amongst Top Three Best Papers, ChipEx, May 2012.
   - DesignVision Award in Semiconductor & IP for Algorithmic Memory, Feb. 2012.
   - Best Paper Award Nominee for Algorithmic Memory, DesignCon, Feb. 2012.
3. MIT Technology Review (TR35) Young Innovator Award, Aug. 2008.
4. ACM Best Doctoral Dissertation Award Nominee, Stanford University, Aug. 2008.
5. Arthur L. Samuel Best Doctoral Thesis Award, Stanford University, July 2008.
6. Cisco Systems FMA Fellowship, Stanford University, 2002-2003.
7. Siebel Scholars Fellowship, Stanford University, Aug. 2001.
8. Selected Amongst Best Papers at IEEE Hot Interconnects, Aug. 2001.
9. Christofer Stephenson Best Masters Thesis Award, Stanford University, Sep. 2000.
10. Indian National Talent Search in Physics (NSEP), 1993.
11. Indian National Maths Olympiad (INMO) Qualifier, 1993.
12. Indian National Talent Search Scholarship, 1992-1998.
13. Indian National Merit Certificate, 1992.

PUBLICATIONS

PAPERS

1. Kartik Mohanram, Sundar Iyer, "MemSecure: Enabling Orders of Magnitude Reduction in Embedded Memory Certification and Trust Effort", *GOMAC Tech*, Mar. 2013.
2. Kartik Mohanram, Mathew Wartell, Sundar Iyer, "MemPack: An Order of Magnitude Reduction in the Cost, Risk, and Time for Memory Compiler Certification", *DATE*, Mar. 2013.
3. Mohammad Alizadeh, Adel Javanmard, Shang-Tse Chuang, Sundar Iyer, Yi Lu, "Versatile Refresh: Low-Complexity Refresh Scheduling for High-throughput Multi-banked eDRAM", *SIGMETRICS*, June 2012.
4. Sundar Iyer, Shang-Tse Chuang, "Algorithmic Memory: An Order of Magnitude Performance Increase for Next Generation SoC", *DesignCon*, Jan. 2012.
5. Sundar Iyer, R. R. Kompella, Nick McKeown, "Designing Packet Buffers for Router Line Cards", *To appear in IEEE/ACM Transactions on Networking*, June 2008.
6. Shang-Tse Chuang, Sundar Iyer, Nick McKeown, "Practical Algorithms for Performance Guarantees in Buffered Crossbars", *IEEE INFOCOM*, March 2005.
7. Sundar Iyer, Nick McKeown, "Analysis of the Parallel Packet Switch Architecture", *IEEE/ACM Transactions on Networking*, vol. 11, no. 2, pp. 314-324, Apr. 2003.
8. Sundar Iyer, Nick McKeown, "Using Constraint Sets to Achieve Delay Bounds in CIOQ Switches", *IEEE Communication Letters*, vol. 7, no. 6, pp. 275-277, Jun. 2003.

9. Sundar Iyer, Supratik Bhattacharrya, Nina Taft, Christophe Diot, "An Approach to Alleviate Link Overload as Observed on an IP Backbone". To appear in *proceedings of IEEE INFOCOM*, San Francisco, March 2003.
10. Sundar Iyer, Rui Zhang, Nick McKeown, "Routers with a Single Stage of Buffering", *Proceedings of ACM SIGCOMM*, Pittsburgh, Pennsylvania, Sep 2002. Also in *Computer Communication Review*, vol. 32, no. 4, Oct 2002.
11. Sundar Iyer, Nick McKeown, "On the Speedup Required for a Multicast Parallel Packet Switch", *IEEE Communication Letters*, June 2001, vol. 5, no. 6, pp. 269-271.
12. Sundar Iyer, Ramana Rao, Nick McKeown, "Analysis of a Memory Architecture for Fast Packet Buffers", *IEEE - High Performance Switching and Routing*, Dallas, May 2001, pp. 368-373.
13. Sundar Iyer, Nick McKeown, "Making Parallel Packet Switches Practical", *Proceedings of IEEE INFOCOM*, Alaska, April 2001, vol. 3, pp. 1680-87.
14. Sundar Iyer, Ramana Rao Kompella, Ajit Shelat, "ClassiPI: An Architecture for Fast and Flexible Packet Classification", *IEEE NETWORK, Special Issue on Fast IP Packet Forwarding and Classification for Next Generation Internet Services*, Mar-Apr. 2001.
15. Sundar Iyer, Ajay Desai, Ajay Tambe, Ajit Shelat, "ClassiPI: A Classifier for Next Generation Policy Based Engines", *IEEE Hot Chips*, Stanford University, Aug 2000.
16. Sundar Iyer, Amr. A. Awadallah, Nick McKeown, "Analysis of a Packet Switch with Memories Running Slower than the Line Rate", *Proceedings of IEEE INFOCOM*, Tel Aviv, March 2000, pp.529-537.

INVITED PAPERS

17. Sundar Iyer, Nick McKeown, "Maximum Size Matchings and Input Queued Switches", *Proceedings of the 40th Annual Allerton Conference on Communication, Control, and Computing*, Monticello, Illinois, Oct 2002.
18. D. Shah, Sundar Iyer, Balaji Prabhakar, Nick McKeown, "Maintaining Statistics Counters in Router Line Cards", *IEEE Micro,* Jan-Feb, 2002, pp. 76-81. Also appeared as "Analysis of a Statistics Counter Architecture" in *IEEE Hot Interconnects*, Stanford University, Aug. 2001.

OTHER REPORTS

19. Shang-Tse Chuang, Sundar Iyer, Nick McKeown, "Practical Algorithms for Performance Guarantees in Buffered Crossbars *Stanford HPNG Technical Report TR03-HPNG-061501*, July 2003.
20. Sundar Iyer, R. R. Kompella, Nick McKeown, "Designing Packet Buffers for Router Line Cards", *Stanford HPNG Technical Report - TR02-HPNG-031001*, Stanford University, Mar. 2002.
21. Sundar Iyer, Supratik Bhattacharrya, Nina Taft, Christophe Diot, "An Approach to Alleviate Link Overload as Observed on an IP Backbone", *Sprint ATLTR02-ATL-071127*, July 2002
22. Sundar Iyer, Supratik Bhattacharrya, Nina Taft, Christophe Diot, "A Measurement Based Study of Load Balancing on an IP Backbone", *Sprint ATL TR02-ATL-051027*, May 2002.
23. Sundar Iyer, Nick McKeown, "Techniques for Fast Shared Memory Switches", *Stanford HPNG Technical Report - TR01-HPNG-081501*, Stanford University, Aug 2001.
24. Sundar Iyer, "The Parallel Packet Switch Architecture", *Masters Thesis Report*, May 2000, Stanford University.

INDUSTRY WORKSHOPS

25. Sundar Iyer,"Algorithmic Memory Increases Memory Performance by an Order of Magnitude, *ChipEx*, April 2012.
26. Sundar Iyer, "Algorithmic Memory Increases Memory Performance by an Order of Magnitude", *Design and Re-use IP SOC*, Shanghai, China, Sep 2012. Also, at *ChipEx*, Tel Aviv, Israel, May 2012.
27. Sundar Iyer, Shang-Tse Chuang, Algorithmic Memory: An Order of Magnitude Performance Increase for Next Generation SoCs, *DesignCon*, Jan. 2012.
28. Sundar Iyer, R.R. Kompella, Nick McKeown, "Techniques for Fast Packet Buffers", *IEEE - GBN Workshop*, Anchorage, Alaska, USA, April 2001.
29. Sundar Iyer, Ajit Shelat, "Requirements for a packet classification API", *Network Processor Forum (CPIX)*, Denver, Colorado - Mar. 2001.
30. Sundar Iyer, Ajit Shelat, "Co-processors and the role of specialized hardware", *NETWORLD + INTEROP*, Las Vegas, Nevada, May 2000.

PATENTS

1. Sundar Iyer, Da Chuang, "System and Method for Storing Data in a Virtualized High Speed Memory System", Memoir Systems, U.S. Patent-8433880.
2. Sundar Iyer, Da Chuang, "System and Method for Storing Data in a Virtualized High Speed Memory System (CIP)", Memoir Systems, U.S. Patent-8266408.
3. Sundar Iyer, Da Chuang, "System and Method for Reduced Latency Caching", Memoir Systems, U.S. Patent-8677072.
4. Sundar Iyer, Sanjeev Joshi, Da Chuang, "Intelligent Memory System Compiler", Memoir Systems, U.S. Patent-8589851
5. Sundar Iyer, Da Chuang, T. Nguyen, S. Joshi, A. Kablanian, "Methods and Apparatus for Designing and Constructing Multi-port Memory Circuits with Voltage Assist", Memoir Systems, U.S. Patent-8760958.
6. Sundar Iyer, Da Chuang, "System and Method for Storing Data in a Virtualized High Speed Memory System with an Integrated Memory Mapping Table", Memoir Systems, U.S. Patent-8504796.
7. Sundar Iyer, Nick McKeown, "High Speed Memory and Input/Output Processor Subsystem for Efficiently Allocating and using High-speed Memory and Slower-speed Memory", Nemo Systems, U.S. Patent-7,657,706.
8. Sundar Iyer, Supratik Bhattacharrya, Nina Taft, Christophe Diot, "Method for Deflection Routing of Data Packet to Alleviate Link Overload in IP Networks", Sprint Labs, U.S. Patent-7362703
9. Sundar Iyer, Ajit Shelat, George Varghese et al., "Fast, Deterministic Exact Match Look-ups In Large Tables", SwitchOn Networks, U.S. Patent-7043494.
10. Sundar Iyer, Ajit Shelat, Raghunath Iyer et al., "Parallel String Pattern Searches in Respective Ones Of Array of Nanocomputers", SwitchOn Networks, U.S. Patent-6631466.
11. Sundar Iyer, Ajit Shelat et al., "Control System for High Speed Rule Processors", SwitchOn Networks, U.S. Patent-6611875.
12. Sundar Iyer, Ajit Shelat et al.,"Method and Apparatus for High-Speed Network Rule Processing using an Array of Cells-I", SwitchOn Networks, U.S. Patent-7136926.
13. Sundar Iyer, Ajit Shelat et al., "Method and Apparatus for High-Speed Network Rule Processing-II", SwitchOn Networks, U.S. Patent-6691168.
14. Sundar Iyer, Ajit Shelat et al.,"Method and Apparatus for High-Speed Network Rule Processing using an Array of Cells-III", SwitchOn Networks, U.S. Patent-6510509.
15. Subhash Bal, Raghunath Iyer, Sundar Iyer, "Method and Apparatus for Performing Internet Network Address Translation", SwitchOn Networks, U.S. Patent-6457061.

PATENT APPLICATIONS

1. Sundar Iyer, Nick McKeown, "High Speed Memory Control and I/O Processor System", Nemo Systems, U.S. Patent App-20050240745.
2. Sundar Iyer, Jeff Chou, Nick McKeown, "High Speed Packet-buffering System", Nemo Systems, U.S. Patent App-11/182,731.
3. Sundar Iyer, Morgan Littlewood, Nick McKeown, "Intelligent Memory Interface", Nemo Systems, U.S. Patent App-11/222,387.
4. Sundar Iyer, Shadab Nazar, Da Chuang, S. Joshi, "Methods and Apparatus for Testing and Repair of Digital Circuits", Memoir Systems, U.S. Patent App.
5. Sundar Iyer, Da Chuang, T. Nguyen, S. Joshi, A. Kablanian, "Methods and Apparatus for Constructing Dual-port Memory by Fusion of Algorithmic and Physical Memory", Memoir Systems, U.S. Patent App.
6. Sundar Iyer, Da Chuang, T. Nguyen, S. Joshi, A. Kablanian, "Methods and Apparatus for Constructing Four-port Memory by Fusion of Algorithmic and Physical Memory", Memoir Systems, U.S. Patent App.
7. Sundar Iyer, Da Chuang, T. Nguyen, S. Joshi, A. Kablanian, "Methods and Apparatus for Constructing multi-port Memory by Fusion of Algorithmic and Physical Memory", Memoir Systems, U.S. Patent App.
8. Sundar Iyer, Da Chuang, "High Speed Memory Systems and Methods for Designing Hierarchical Memory Systems", Memoir Systems, U.S. Patent App.
9. Sundar Iyer, Da Chuang, T. Nguyen, S. Joshi, A. Kablanian, "Methods and Apparatus for Designing and Constructing High-speed Memory Circuits", Memoir Systems, U.S. Patent App.
10. Sundar Iyer, Da Chuang, T. Nguyen, S. Joshi, A. Kablanian, "Methods and Apparatus for Designing and Constructing Multi-port Memory Circuits with Voltage Assist", Memoir Systems, U.S. Patent App.
11. Kartik Mohanram, Sharad Chole, Sameek Banerjee, Sreenivas Reddy, Sundar Iyer, "Methods and Apparatus for Constructing Algorithmic Ternary Content Addressable Memory Circuits (TCAMs)", U.S. Patent App.

TALKS

1. Sundar Iyer,"Algorithmic Memory: An Order of Magnitude Increase in Next Generation Embedded Memory Performance", *IBM STS Meet*, Dec 2013.
2. "Analysing Internet Routers with Pigeons", Cisco Systems, Technology Seminar, Jan. 2008.
3. "Network Memory Technology", D.E and Fellows Seminar, Cisco Systems, Apr. 2006.
4. "Caching Algorithms for Network Buffers", Comp. Arch. Seminar, Stanford University, Nov. 2005.
5. "Practical Algorithms for Performance Guarantees in Buffered Crossbars", Stanford Networking Seminar, California, Jan. 2003.
6. "Analyzing CIOQ Switches using the Constraint Set Technique", Stanford University, California, Feb. 2002.
7. "Analysis of the Parallel Packet Switch Architecture", Dept. of EE, I. I. T. Bombay, India - Dec. 2001.
8. "Designing Packet Buffers for Networking", Rambus Inc. (Apr. 2001, Sep. 2002), Infineon Technologies (Apr. 2002, May 2002), Juniper Networks (Apr. 2001), University of California Davis (Oct 2002).
9. "Shortest Path Routing via Alternate Nearest Neighbor", Sprint ATL Research Seminar, Lake Tahoe, California, Mar. 2002.
10. "Some Observations towards Load Balancing over a Network", Sprint ATL Research Seminar, San Francisco, California, Aug. 2001.

PROFESSIONAL ACTIVITIES

1. Guest Lecturer for Advanced Graduate Courses on Packet Switching Architectures, EE384X, EE384Y, Stanford University, 2012.
2. Guest Lecturer for EE203, The Entrepreneurial Engineer, Stanford University, Feb 2012.
3. Guest Lecturer for EE Seminar on Entreprenuership, Stanford University, 2008.
4. Guest Lecturer for Advanced Graduate Courses on Packet Switching Architectures, EE384X, EE384Y, Stanford University, 2006.
5. Technical Program Committee Member, QoS-IP, Milano, Italy, 2003.
6. Member Network Processing Forum (Originally CPIX) - 2000-2001.
7. Reviewer (Journals) - *IEEE/ACM Transactions on Networking, IEEE Journal on Selected Areas in Communications, IEEE Network, Computer Networks, IEEE Comm. Letters, Journal of High Speed Networks.*
8. Reviewer (Conferences) - *IEEE INFOCOM, ACM SIGCOMM, IEEE Hot Interconnects, IEEE Globecom, ACM SIGMETRICS, ISCA, IEEE HPSR, USENIX NSDI.*
9. Guest Lecturer for Computer Networks, Center for Development of Advanced Computing (CDAC), MET Mumbai, 1997.

OTHER

- *Languages:* Proficient in English, Hindi and Marathi. Working knowledge of Tamil and German.
- *Activities:* Ballroom Dance (Competitive Bronze Level II-III), Guitar, Fiction Writing.
- *Sports:* Swimming, Tennis, Chess.
- *Hobbies:* Improv, Recreational Mathematics.
- *Service:* IIT Bombay H8 General Secretary ('96-97), General Councillor ('97-98).
- *Service Award:* IIT Bombay H8 Roll of Honor (1998).