

SUNDAR IYER

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PARTICULARS

EDUCATION

Stanford University Ph. D. Candidate in Computer Science [†] <i>Thesis: Load Balancing and Parallelism for the Internet</i>	Stanford, CA <i>Defended Feb '03, Expected June '08</i>
Stanford University M. S. in Computer Science <i>Distinction in Research</i>	Stanford, CA <i>June 2000</i>
Indian Institute of Technology (I. I. T.), Bombay B. Tech. in Computer Science and Engineering	Mumbai, India <i>April 1998</i>

ENTREPRENEURSHIP

- **CTO, Co-Founder and Member of the Board, Nemo Systems**, Nov 2003 - Sep 2005. Nemo Systems (acquired by Cisco Systems in Sep 2005) was a fabless semiconductor company, building caching technologies for scaling high-speed networking systems. Founded the company based on the mathematical work done during my Ph.D. thesis. Responsible for customer and technology strategy, algorithm development and intellectual property. Company was venture backed, had a team of 6 employees, and raised \$1.8 million in venture financing.
- **Senior Systems Architect, Founding Member, SwitchOn Networks**, Jan. 1999 - Sep. 2000. Part of the initial founding team of six at SwitchOn Networks. Company grew to 50+ employees and was later acquired by PMC-Sierra in Sep. 2000. Jointly responsible for the system architecture and algorithm development for deep packet classification. The company commercialized, ClassiPI, a content hardware co-processor for Internet routers in Feb. 2001. Primarily responsible for the company's patent strategy. Other joint responsibilities included technical marketing, venture interaction, and sales.

WORK EXPERIENCE

- **Technical Leader, Cisco Systems**, Oct 2005 - Current. I co-lead the Network Memory Group, which is focussed on the deployment of the memory caching, intelligence and serialization technology after the acquisition of Nemo Systems. Developed architectural solutions, memory ASICs, caching and load-balancing algorithms; lead architecture, patent strategy and technology evaluation. Facilitated the use of the technology on Cisco's high-speed enterprise and core switching products at speeds ranging between 20-80Gb/s. The technology is being deployed on 21 unique instances, on more than 10 of Cisco's high-speed enterprise routers, with 6M+ instances per annum of the technology in deployment by 2009. Negotiated financing from Cisco's central development organization (CDO) in August 2007, to proliferate the technology widely across the campus, core, enterprise and Internet router infrastructure. Currently lead a team of 13 engineers and drive Cisco's smart memory initiative to scale the performance of networking systems beyond 100Gb/s line rates.
- **Consultant, Nevis Networks Inc.**, Sep. 2003 - Mar 2004. Analyzed the performance of the Nevis switch fabric. Suggested theoretically optimal and practical packet switching algorithms for the distributed shared memory switch fabric.
- **Systems Engineer, PMC-Sierra**, Sep. 2000 - Oct. 2001. Involved with the architecture and algorithms for the next generation of a deep packet classification device.
- **Consultant, RIMO Technologies, India**, Jun. 1998 - Dec. 1998.

[†]On leave of absence from March 2003 to March 2008.

HONORS & PRIZES

- Cisco Systems FMA Fellowship, Stanford University, 2002-2003.
- Siebel Scholars Fellowship, Stanford University, 2001.
- Christofer Stephenson Memorial Award for the best Masters Thesis in Computer Science, Stanford, 2000.
- Paper chosen amongst the best papers from IEEE Hot Interconnects 2001.
- Indian National Talent Search Merit Scholarship, 1992-1998.
- Indian National Talent Search Examination in Physics (NSEP) awardee, 1993.
- Selected to participate in the Indian National Maths Olympiad, 1993.
- Indian National Merit Scholarship, 1992-1998.

PUBLICATIONS

PAPERS

1. Sundar Iyer, R. R. Kompella, Nick McKeown, "Designing Packet Buffers for Router Line Cards", *To appear in IEEE/ACM Transactions on Networking*, June 2008.
2. Shang-Tse Chuang, Sundar Iyer, Nick McKeown, "Practical Algorithms for Performance Guarantees in Buffered Crossbars", *IEEE INFOCOM 2005*.
3. Sundar Iyer, Nick McKeown, "Analysis of the Parallel Packet Switch Architecture", *IEEE/ACM Transactions on Networking*, vol. 11, no. 2, pp. 314-324., Apr. 2003.
4. Sundar Iyer, Nick McKeown, "Using Constraint Sets to Achieve Delay Bounds in CIOQ Switches", *IEEE Communication Letters*, vol. 7, no. 6, pp. 275-277., Jun. 2003.
5. Sundar Iyer, Supratik Bhattacharyya, Nina Taft, Christophe Diot, "An Approach to Alleviate Link Overload as Observed on an IP Backbone". To appear in *proceedings of IEEE INFOCOM*, San Francisco, March 2003. A more detailed version of this paper appears in two technical reports as, "An Approach to Alleviate Link Overload as Observed on an IP Backbone", *Sprint ATL TR02-ATL-071127*, July 2002 and "A Measurement Based Study of Load Balancing on an IP Backbone", *Sprint ATL TR02-ATL-051027*, May 2002.
6. Sundar Iyer, Rui Zhang, Nick McKeown, "Routers with a Single Stage of Buffering", *Proceedings of ACM SIGCOMM*, Pittsburgh, Pennsylvania, Sep 2002. Also in *Computer Communication Review*, vol. 32, no. 4, Oct 2002.
7. Sundar Iyer, Nick McKeown, "On the Speedup Required for a Multicast Parallel Packet Switch", *IEEE Communication Letters*, June 2001, vol. 5, no. 6, pp. 269-271.
8. Sundar Iyer, Ramana Rao, Nick McKeown, "Analysis of a Memory Architecture for Fast Packet Buffers", *IEEE - High Performance Switching and Routing*, Dallas, May 2001, pp. 368-373. A more detailed version of this work was presented in the *IEEE GBN Workshop*, Alaska, April 2001.
9. Sundar Iyer, Nick McKeown, "Making Parallel Packet Switches Practical", *Proceedings of IEEE INFOCOM*, Alaska, April 2001, vol. 3, pp. 1680-87.
10. Sundar Iyer, Ramana Rao Kompella, Ajit Shelat, "ClassiPI: An Architecture for Fast and Flexible Packet Classification", *IEEE NETWORK, Special Issue on Fast IP Packet Forwarding and Classification for Next Generation Internet Services*, Mar-Apr. 2001.
11. Sundar Iyer, Ajay Desai, Ajay Tambe, Ajit Shelat, "ClassiPI: A Classifier for Next Generation Policy Based Engines", *IEEE Hot Chips*, Stanford University, Aug 2000.
12. Sundar Iyer, Amr. A. Awadallah, Nick McKeown, "Analysis of a Packet Switch with Memories Running Slower than the Line Rate", *Proceedings of IEEE INFOCOM*, Tel Aviv, March 2000, pp.529-537.

INVITED PAPERS

13. Sundar Iyer, Nick McKeown, "Maximum Size Matchings and Input Queued Switches", *Proceedings of the 40th Annual Allerton Conference on Communication, Control, and Computing*, Monticello, Illinois, Oct 2002.
14. D. Shah, Sundar Iyer, Balaji Prabhakar, Nick McKeown, "Maintaining Statistics Counters in Router Line Cards", *IEEE Micro*, Jan-Feb, 2002, pp. 76-81. Also appeared as "Analysis of a Statistics Counter Architecture" in *IEEE Hot Interconnects*, Stanford University, Aug. 2001.
15. "Maintaining State in Router Line Cards", with Nick McKeown. In preparation for *IEEE Communication Letters*.

OTHER REPORTS

16. Sundar Iyer, Nick McKeown "Techniques for Fast Shared Memory Switches", *HPNG Technical Report - TR01-HPNG-081501*, Stanford University, Aug 2001.
17. Sundar Iyer, "The Parallel Packet Switch Architecture", *Masters Thesis Report*, May 2000, Stanford University.

PATENTS & APPLICATIONS

1. Multiple patent applications in progress for various algorithms and techniques for the design of network memory, new caching algorithms for packet scheduling, storage, VOQ buffering, policing, power reduction, redundancy, and memory serialization protocols.
2. Sundar Iyer, Nick McKeown., “High speed memory control and I/O processor system”. U.S. Patent App Num-20050240745.
3. Sundar Iyer, Jeff Chou, Nick McKeown., “High speed packet-buffering System”. U.S. Patent App-11/182,731.
4. Sundar Iyer, Morgan Littlewood, Nick McKeown., “Intelligent Memory Interface”. U.S. Patent App-11/222,387.
5. Sundar Iyer, Supratik Bhattacharya, Nina Taft, Christophe Diot, “A Method to Alleviate Link Overload on an IP Backbone”.
6. Sundar Iyer, Ajit Shelat, George Varghese et al., “Fast, Deterministic Exact Match Look-ups In Large Tables”. U.S. Patent-7043494.
7. Sundar Iyer, Ajit Shelat, Raghunath Iyer et al., “Parallel string pattern searches in respective ones of array of nanocomputers”. U.S. Patent-6631466.
8. Sundar Iyer, Ajit Shelat et al., “Control System for High Speed Rule Processors”. U.S. Patent-6611875.
9. Sundar Iyer, Ajit Shelat et al., “Method and Apparatus for High-Speed Network Rule Processing using an Array of Cells-I”. U.S. Patent-7136926.
10. Sundar Iyer, Ajit Shelat et al., “Method and Apparatus for High-Speed Network Rule Processing-II”. U.S. Patent-6691168.
11. Sundar Iyer, Ajit Shelat et al., “Method and Apparatus for High-Speed Network Rule Processing using an Array of Cells-III”. U.S. Patent-6510509.
12. Subhash Bal, Raghunath Iyer, Sundar Iyer, “Method and Apparatus for Performing Internet Network Address Translation”, U.S. Patent-6457061.

TALKS

1. “Analysing Internet Routers with Pigeons”, Cisco Systems, Technology Seminar, Jan. 2008.
2. *(Invited)* “Network Memory Technology”, Fellows and Distinguished Engineers Meet, Cisco Systems, Apr. 2006.
3. “Caching Algorithms for Network Buffers”, Computer Architecture Seminar, Stanford University, Nov. 2005.
4. “An Approach to Alleviate Link Overload as Observed on an IP Backbone”, *IEEE INFOCOM 2003*, San Francisco, California, Apr. 2003.
5. “Practical Algorithms for Performance Guarantees in Buffered Crossbars”, Stanford Networking Seminar, California, Jan. 2003.
6. *(Invited)* “Maximum Size Matchings and Input Queued Switches”, *40th Annual Allerton Conference on Communication, Control, and Computing*, Monticello, Illinois, Oct. 2002.
7. “Routers with a Single Stage of Buffering”, *ACM SIGCOMM*, Pittsburgh, Pennsylvania, Aug 2002.
8. “Shortest Path Routing via Alternate Nearest Neighbor”, Sprint ATL Retreat, Lake Tahoe, California, Mar. 2002.
9. “Analyzing CIOQ Switches using the Constraint Set Technique”, Stanford University, California, Feb. 2002.
10. “Some Observations towards Load Balancing over a Network”, Sprint ATL Retreat, San Francisco, California, Aug. 2001.
11. “Analysis of a Statistics Counter Architecture”, *IEEE Hot Interconnects*, Stanford, California, Aug. 2001.
12. “Analysis of a Memory Architecture for Fast Packet Buffers”, *IEEE - High Performance Switching and Routing*, Dallas, Texas, May 2001.
13. *(various venues)* “Designing Packet Buffers for Networking”,
 - Rambus Inc., Los Altos, California - Apr. 2001, Sep. 2002.
 - Infineon Technologies, San Jose, California - Apr. 2002, May 2002.
 - Juniper Networks, Sunnyvale, California - Apr. 2001.
 - University of California Davis, Davis, California - Oct 2002.
14. “Making Parallel Packet Switches Practical”, *IEEE INFOCOM 2001*, Anchorage, Alaska, USA, April 2001.
15. “Techniques for Fast Packet Buffers”, *IEEE - GBN Workshop 2001*, Anchorage, Alaska, USA, April 2001.
16. “Requirements for a packet classification API”, Network Processor Forum (CPIX), Denver, Colorado - Mar. 2001.

17. "ClassiPI: A Classifier for Next Generation Content/Policy Based Switches", *IEEE Hotchips*, Stanford, California, August 2000.
18. "Co-processors and the role of specialized hardware", *NETWORLD + INTEROP 2000*, Las Vegas, Nevada, May 2000.
19. "Analysis of a Packet Switch with memories running slower than the line-rate", *IEEE INFOCOM 2000*, Tel Aviv, Israel, March 2000.
20. (*various venues*) "Analysis of the Parallel Packet Switch Architecture",
 - (*Invited*) Dept. of Electrical Engineering, I. I. T. Bombay, India - Dec. 2001.
 - SwitchOn Networks, Pune, India - Sep. 1999.

PROFESSIONAL ACTIVITIES

- Technical Program Committee Member, QoS-IP, Milano, Italy, 2003.
- Member Network Processing Forum (Originally CPIX) - 2000-2001.
- Reviewer (Journals) - *IEEE/ACM Transactions on Networking*, *IEEE Journal on Selected Areas in Communications*, *IEEE Network*, *Computer Networks*, *IEEE Communication Letters*, *Journal of High Speed Networks*. (Conferences) - *IEEE INFOCOM*, *ACM SIGCOMM*, *IEEE Hot Interconnects*, *IEEE Globecom*, *ACM SIGMETRICS*, *ISCA*, *IEEE HPSR*
- Teaching Assistant and Guest Lecturer for advanced graduate courses on Packet Switching Architectures-I and II at Stanford University.
- Co-teacher for Computer Networks, Center for Development of Advanced Computing (CDAC) at MET Mumbai.

OTHER

- *Languages*: Proficient in English, Hindi and Marathi. Working knowledge of Tamil and German.
- *Activities*: Ballroom Dance (Bronze Level II-III), Guitar, Singing, Music Composition.
- *Sports*: Swimming, Triathlon, Tennis, Chess.
- *Hobbies*: Standup Comedy, Recreational Math.